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DATA SHEET

SAA1575HL
Global Positioning System (GPS) baseband processor

Product specification
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Philips Semiconductors

PHILIPS

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1 FEATURES

- Single-chip GPS baseband solution with built-in 16-bit microcontroller
- All digital, 0.5 micron CMOS technology
- Single power supply with full 3 V operation
- Separate I/O power supply pins for operation with 3 or 5 V external devices
- Up to 30 MHz system clock from on-chip crystal oscillator or external clock input
- 2 kbytes words internal data memory for fast execution
- External bus for up to 512 kbytes words data memory and 512 kbytes words program memory
- Programmable external bus timing to match external memory speed
- Chip selection outputs to reduce glue logic requirements
- Reset controller for power-down detection and servicing
- 8 GPS channel correlators driven by firmware for flexible GPS correlation algorithms
- 1 second pulse output of GPS time
- 2-bit digital IF GPS signal input synchronized to external sample clock
- 2 fully duplex UARTs for communication with host system processor and other devices
- Real-time clock with 32.768 kHz crystal and supply for low power timekeeping
- Watchdog timer
- Power-down modes under firmware control
- 100-pin LQFP package
- 50 mA supply current (typ.) when 8 GPS channels in track (approximate).

2 GENERAL DESCRIPTION

The SAA1575HL is an integrated circuit which implements a complete baseband function for Global Positioning System (GPS) receivers. It combines a 16-bit Philips 80C51XA microcontroller, 8 GPS channel correlators and related peripherals in a single IC. Users can implement a complete GPS receiver using only the SAA1575HL, the UAA1570HL front-end Philips IC (or similar), external memory and a few discrete components.

The IC is aimed at low cost applications. A low power solution was also used where possible, although this was of secondary importance to cost. The core of the SAA1575HL operates at 3 V.

However, for compatibility with current automotive applications, the periphery is supplied from separate pins and can be operated between 3 and 5 V, as required.

The function of the SAA1575HL is to read the 1 or 2-bit sampled IF bitstream from a front-end IC and, under control of firmware on an external ROM, calculate the full GPS solution. The results are communicated to a host in National Maritime Electronics Association (NMEA) format via a standard serial port. A second serial port can be used to provide differential GPS information to the processor for more advance applications. In addition, various other functions are integrated onto the IC such as a real-time GPS clock, a power-down/reset controller, timer/counters and a watchdog timer.

To summarise, the SAA1575HL has the following functional units:

- 16-bit 80C51XA microcontroller core
- 2 kbytes words on-chip SRAM (16-bit words)
- 8 GPS channel correlators
- 2 UARTs
- 8 general purpose I/O lines
- 3 timer/counters
- 1 real-time clock
- 1 watchdog timer
- 1 power-down/reset controller.

The structure is based on a 16-bit microcontroller core operating on all other units as memory mapped peripherals and registers. A 16-bit data bus and a 19-bit address bus are extended to external pins so that external data and program memory can be accessed. On-chip decoder circuits eliminate the need for external glue logic for external memory access.

Each of the 8 GPS channel correlators includes a carrier Numerically Controlled Oscillator (NCO), PN code generator, phase rotator and low-pass filter. They correlate the local PN sequence with the digitized input GPS signal and generate the filtered correlation result for the microcontroller. The firmware provided then generates a navigation solution and provides standard GPS data outputs to the user.

The GPS firmware is located in off-chip program memory. It processes the GPS signals from up to 8 satellites and generates GPS information that can be output to the host processor through one of the two serial ports. Much of hardware configuration of the SAA1575HL can be controlled by the firmware and so details such as the external bus timing may change between firmware revisions. For the purpose of this document, the standard Philips firmware has been assumed (release HD00).

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC(core)}$	core supply voltage		2.7	3.3	3.6	V
$V_{CC(P)}$	peripheral supply voltage		2.7	5.0	5.5	V
$V_{CC(R)}$	real-time clock core supply voltage		2.4	3.3	3.6	V
$V_{CC(B)}$	backup peripheral supply voltage		2.7	5.0	5.5	V
$I_{CC(core)}$	core supply current	normal mode	–	35	–	mA
		sleep mode	–	15	–	mA
$I_{CC(R)}$	real-time clock core supply current	f_{RTC} = 32.768 kHz	–	10	30	µA
$I_{CC(B)}$	backup peripheral supply current	normal mode; dependent on load	–	5	–	mA
		sleep mode	–	1	–	µA
$I_{CC(P)}$	peripheral supply current	normal mode	–	20	–	mA
		sleep mode	–	–	1	mA
f_{osc}	oscillator frequency		26	30	32	MHz
T_{amb}	ambient temperature		–40	+25	+85	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA1575HL	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

5 BLOCK DIAGRAM

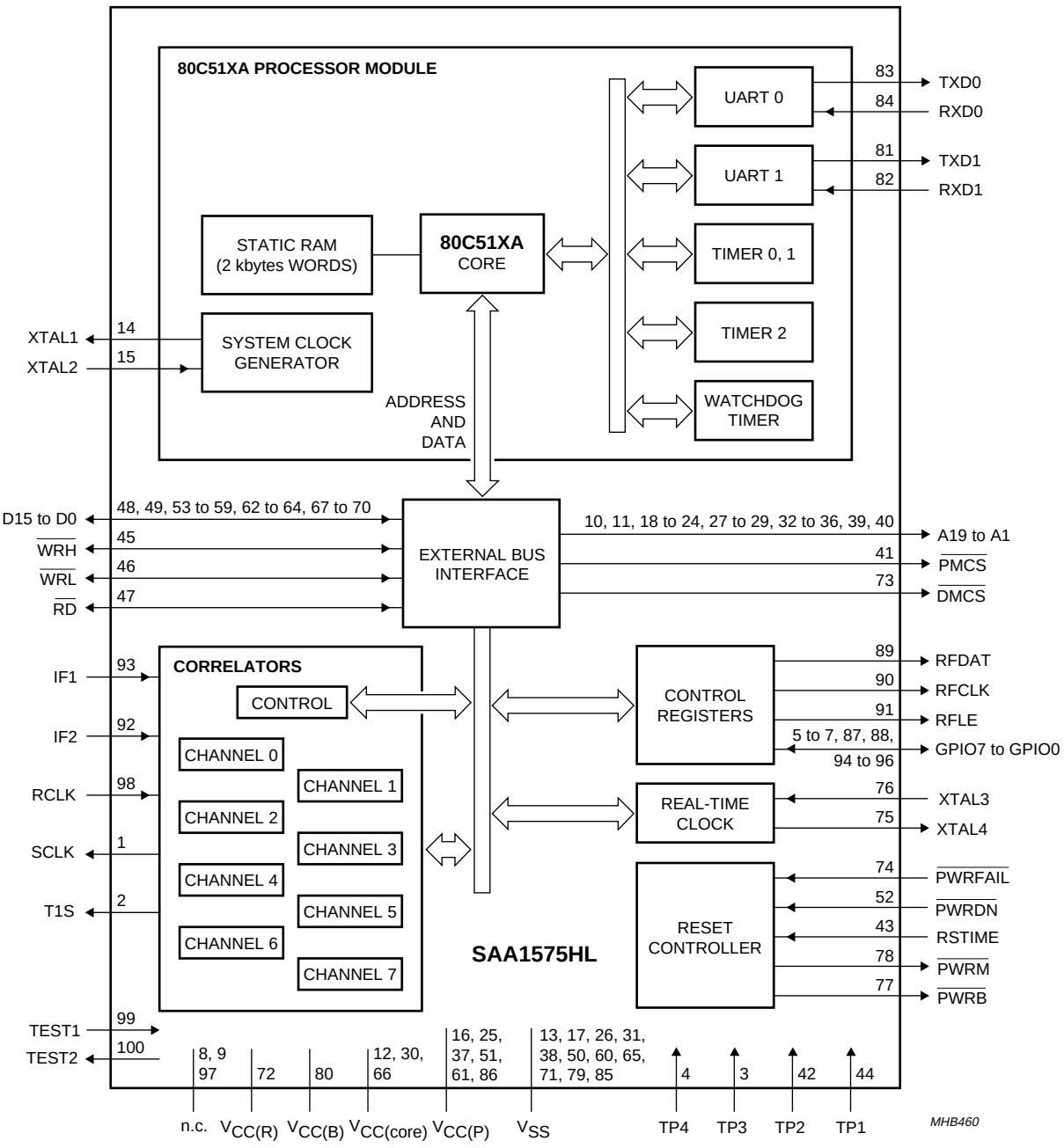


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
SCLK	1	O	**Sample clock**: sample clock generated internally by dividing down the RCLK (reference clock) input. This output is provided for use by the front-end IC.
T1S	2	O	**GPS time pulse**: a 1 pulse per second output whose rising or falling edge (firmware controlled) is synchronized to GPS time when the receiver is tracking a GPS signal. The pulse length is approximately 1 ms.
TP3	3	I	**Test pin**: tie HIGH
TP4	4	I	**Test pin**: tie HIGH
GPIO5	5	I/O	**GPIO bit 5**: standard general purpose I/O mapped into the segment 15 of the address space. The top 4 bits can be used as the XA external timer control access pins (T0, T1, T2 and T2EX).
GPIO6	6	I/O	**GPIO bit 6**: standard general purpose I/O mapped into the segment 15 of the address space. The top 4 bits can be used as the XA external timer control access pins (T0, T1, T2 and T2EX).
GPIO7	7	I/O	**GPIO bit 7**: standard general purpose I/O mapped into the segment 15 of the address space. The top 4 bits can be used as the XA external timer control access pins (T0, T1, T2 and T2EX).
n.c.	8	O	**Not connected**: do not connect
n.c.	9	O	**Not connected**: do not connect
A19	10	O	**External memory address bus bit 19**: 19-bit address bus; used to address external RAM and program memory
A18	11	O	**External memory address bus bit 18**: 19-bit address bus; used to address external RAM and program memory
$V_{CC(core)}$	12	–	**Main core power supply**: 2.7 to 3.6 V only; main supply for the core in normal operation
V_{SS}	13	–	**Ground**: 0 V reference
XTAL1	14	I	**Crystal 1**: input to the inverting amplifier; used in the system oscillator circuit and input to the internal clock generator circuits
XTAL2	15	O	**Crystal 2**: output from the system oscillator amplifier
$V_{CC(P)}$	16	–	**Main I/O power supply**: 2.7 to 5.5 V operating range; main supply for the periphery in normal operation
V_{SS}	17	–	**Ground**: 0 V reference
A17	18	O	**External memory address bus bit 17**: 19-bit address bus; used to address external RAM and program memory
A16	19	O	**External memory address bus bit 16**: 19-bit address bus; used to address external RAM and program memory
A15	20	O	**External memory address bus bit 15**: 19-bit address bus; used to address external RAM and program memory
A14	21	O	**External memory address bus bit 14**: 19-bit address bus; used to address external RAM and program memory
A13	22	O	**External memory address bus bit 13**: 19-bit address bus; used to address external RAM and program memory
A12	23	O	**External memory address bus bit 12**: 19-bit address bus; used to address external RAM and program memory

SYMBOL	PIN	I/O	DESCRIPTION
A11	24	O	**External memory address bus bit 11**: 19-bit address bus; used to address external RAM and program memory
$V_{CC(P)}$	25	–	**Main I/O power supply**: 2.7 to 5.5 V operating range; main supply for the periphery in normal operation
V_{SS}	26	–	**Ground**: 0 V reference
A10	27	O	**External memory address bus bit 10**: 19-bit address bus; used to address external RAM and program memory
A9	28	O	**External memory address bus bit 9**: 19-bit address bus; used to address external RAM and program memory
A8	29	O	**External memory address bus bit 8**: 19-bit address bus; used to address external RAM and program memory
$V_{CC(core)}$	30	–	**Main core power supply**: 2.7 to 3.6 V only; main supply for the core in normal operation
V_{SS}	31	–	**Ground**: 0 V reference
A7	32	O	**External memory address bus bit 7**: 19-bit address bus; used to address external RAM and program memory
A6	33	O	**External memory address bus bit 6**: 19-bit address bus; used to address external RAM and program memory
A5	34	O	**External memory address bus bit 5**: 19-bit address bus; used to address external RAM and program memory
A4	35	O	**External memory address bus bit 4**: 19-bit address bus; used to address external RAM and program memory
A3	36	O	**External memory address bus bit 3**: 19-bit address bus; used to address external RAM and program memory
$V_{CC(P)}$	37	–	**Main I/O power supply**: 2.7 to 5.5 V operating range; main supply for the periphery in normal operation
V_{SS}	38	–	**Ground**: 0 V reference
A2	39	O	**External memory address bus bit 2**: 19-bit address bus; used to address external RAM and program memory
A1	40	O	**External memory address bus bit 1**: 19-bit address bus; used to address external RAM and program memory
$\overline{PMCS}$	41	O	**External program memory select**: external program memory read strobe
TP2	42	I	**Test pin**: tie LOW
RSTIME	43	I	**Reset timer control**: this controls the on-chip reset timer. If this is HIGH, reset will be de-asserted approximately 10 ms after both $\overline{PWRDN}$ and $\overline{PWRFAIL}$ go HIGH. If this is LOW, reset will be de-asserted approximately 10 μs after both $\overline{PWRDN}$ and $\overline{PWRFAIL}$ go HIGH.
TP1	44	I	**Test pin**: tie LOW
$\overline{WRH}$	45	I/O	**Write MSB**: write strobe for external data memory; asserted for both MSB and word write operations; input mode only used for test purposes
$\overline{WRL}$	46	I/O	**Write LSB**: write strobe for external data memory; asserted for both LSB and word write operations; input mode only used for test purposes
$\overline{RD}$	47	I/O	**External data read**: read strobe for external data memory; input mode only used for test purposes

SYMBOL	PIN	I/O	DESCRIPTION
D15	48	I/O	**External memory data bus**: 16-bit data bus; used to connect to external RAM and program memory
D14	49	I/O	**External memory data bus bit 14**: 16-bit data bus; used to connect to external RAM and program memory
V_{SS}	50	–	**Ground**: 0 V reference
$V_{CC(P)}$	51	–	**Main I/O power supply**: 2.7 to 5.5 V operating range; main supply for the periphery in normal operation
$\overline{PWRDN}$	52	I	**Power-down indicator**: a LOW on this pin asserts an XA interrupt intended for use as a power fail interrupt. Once reset is asserted, either by $\overline{PWRFAIL}$ or the firmware, it will remain asserted until a set time after this pin goes HIGH.
D13	53	I/O	**External memory data bus bit 13**: 16-bit data bus; used to connect to external RAM and program memory
D12	54	I/O	**External memory data bus bit 12**: 16-bit data bus; used to connect to external RAM and program memory
D11	55	I/O	**External memory data bus bit 11**: 16-bit data bus; used to connect to external RAM and program memory
D10	56	I/O	**External memory data bus bit 10**: 16-bit data bus; used to connect to external RAM and program memory
D9	57	I/O	**External memory data bus bit 9**: 16-bit data bus; used to connect to external RAM and program memory
D8	58	I/O	**External memory data bus bit 8**: 16-bit data bus; used to connect to external RAM and program memory
D7	59	I/O	**External memory data bus bit 7**: 16-bit data bus; used to connect to external RAM and program memory
V_{SS}	60	–	**Ground**: 0 V reference
$V_{CC(P)}$	61	–	**Main I/O power supply**: 2.7 to 5.5 V operating range; main supply for the periphery in normal operation
D6	62	I/O	**External memory data bus bit 6**: 16-bit data bus; used to connect to external RAM and program memory
D5	63	I/O	**External memory data bus bit 5**: 16-bit data bus; used to connect to external RAM and program memory
D4	64	I/O	**External memory data bus bit 4**: 16-bit data bus; used to connect to external RAM and program memory
V_{SS}	65	–	**Ground**: 0 V reference
$V_{CC(core)}$	66	–	**Main core power supply**: 2.7 to 3.6 V only; main supply for the core in normal operation
D3	67	I/O	**External memory data bus bit 3**: 16-bit data bus; used to connect to external RAM and program memory
D2	68	I/O	**External memory data bus bit 2**: 16-bit data bus; used to connect to external RAM and program memory
D1	69	I/O	**External memory data bus bit 1**: 16-bit data bus; used to connect to external RAM and program memory
D0	70	I/O	**External memory data bus bit 0**: 16-bit data bus; used to connect to external RAM and program memory
V_{SS}	71	–	**Ground**: 0 V reference

SYMBOL	PIN	I/O	DESCRIPTION
$V_{CC(R)}$	72	–	**Backup core power supply**: 2.4 to 3.6 V only. Separate from the core supply to allow a low capacity battery to be used to maintain the Real-Time Clock (RTC) function. This should be powered from the main supply during normal operation and switched to battery backup when the main supply fails.
$\overline{DMCS}$	73	O	**External data memory select**: external RAM select pin, active LOW when the external data memory space is addressed. This output is driven from $V_{CC(R)}$ and $V_{CC(B)}$ supplies to ensure that the external RAM is not enabled during power-down.
$\overline{PWRFAIL}$	74	I	**Power fail indicator**: a LOW on this pin forces the embedded microcontroller into reset. Reset will not be de-asserted until a set time after both $\overline{PWRDN}$ and $\overline{PWRFAIL}$ go HIGH. For correct start-up, this pin should be LOW on power-up.
XTAL4	75	O	**Crystal 4**: output from the RTC oscillator amplifier; this pin is only 3 V tolerant
XTAL3	76	I	**Crystal 3**: input to inverting amplifier used in the RTC oscillator circuits (32.768 kHz); this pin is only 3 V tolerant
$\overline{PWRB}$	77	O	**Backup supply select**: this output is intended to drive an external FET used to switch the battery backup supply(s). It is active LOW and is controlled directly by the $\overline{PWRFAIL}$.
$\overline{PWRM}$	78	O	**Main supply select**: this output is intended to drive an external FET used to switch the main supply(s). It is active LOW and is controlled directly by $\overline{PWRFAIL}$.
V_{SS}	79	–	**Ground**: 0 V reference
$V_{CC(B)}$	80	–	**Backup I/O power supply**: 2.4 to 5.5 V only. Supply for the RAM select, power fail and power switching I/O pads only allowing these functions to be powered when the main power supply fails. This should be powered from the main supply during normal operation and switched to battery backup when the main supply fails.
TXD1	81	O	**Transmitter output 1**: transmit channel for serial port 1 (UART1) of the embedded processor
RXD1	82	I	**Receiver input 1**: receive channel for serial port 1 (UART1) of the embedded processor. It is intended that this serial port is dedicated to differential GPS information (dependent on firmware).
TXD0	83	O	**Transmitter output 0**: transmit channel for serial port 0 (UART0) of the embedded processor.
RXD0	84	I	**Receiver input 0**: receive channel for serial port 0 (UART0) of the embedded processor. It is intended that this serial port is dedicated to the NMEA data stream (dependent on firmware).
V_{SS}	85	–	**Ground**: 0 V reference
$V_{CC(P)}$	86	–	**Main I/O power supply**: 2.7 to 5.5 V operating range; main supply for the periphery in normal operation
GPIO4	87	I/O	**GPIO bit 4**: standard general purpose I/O mapped into the segment 15 of the address space. The top 4 bits can be used as the XA external timer control access pins (T0, T1, T2 and T2EX).
GPIO3	88	I/O	**GPIO bit 3**: standard general purpose I/O mapped into the segment 15 of the address space. The top 4 bits can be used as the XA external timer control access pins (T0, T1, T2 and T2EX).
RFDAT	89	O	**RFIC set-up data**: serial data output used to set up the UAA1570HL front-end IC.
RFCLK	90	O	**RFIC set-up data**: clock output for the serial data output used to set up the UAA1570HL front-end IC. The state of the RFDAT and RFLE lines is latched into the front-end IC on the rising edge.

SYMBOL	PIN	I/O	DESCRIPTION
RFLE	91	O	**RFIC setup latch**: output used to latch the RFIC set-up into the active UAA1570HL control registers
IF2	92	I	**MSB IF input**: MSB of the 2-bit GPS digital IF signal input. Clocked in on the rising edge of SCLK. If only a 1-bit IF input is available this input should be held HIGH.
IF1	93	I	**LSB IF input**: LSB of the 2-bit GPS digital IF signal input. Clocked in on the rising edge of SCLK.
GPIO2	94	I/O	**GPIO bit 2**: standard general purpose I/O mapped into the segment 15 of the address space. The top 4 bits can be used as the XA external timer control access pins (T0, T1, T2 and T2EX).
GPIO1	95	I/O	**GPIO bit 1**: standard general purpose I/O mapped into the segment 15 of the address space. The top 4 bits can be used as the XA external timer control access pins (T0, T1, T2 and T2EX).
GPIO0	96	I/O	**GPIO bit 0**: standard general purpose I/O mapped into the segment 15 of the address space. The top 4 bits can be used as the XA external timer control access pins (T0, T1, T2 and T2EX).
n.c.	97	O	**Not connected**: do not connect
RCLK	98	I	**Reference clock**: input from the TXCO reference. Not used internally. This is divided under firmware control to produce the sample clock, SCLK, used to gate the IF inputs.
TEST1	99	I	**Test pin**: connect to pin 100
TEST2	100	O	**Test pin**: connect to pin 99

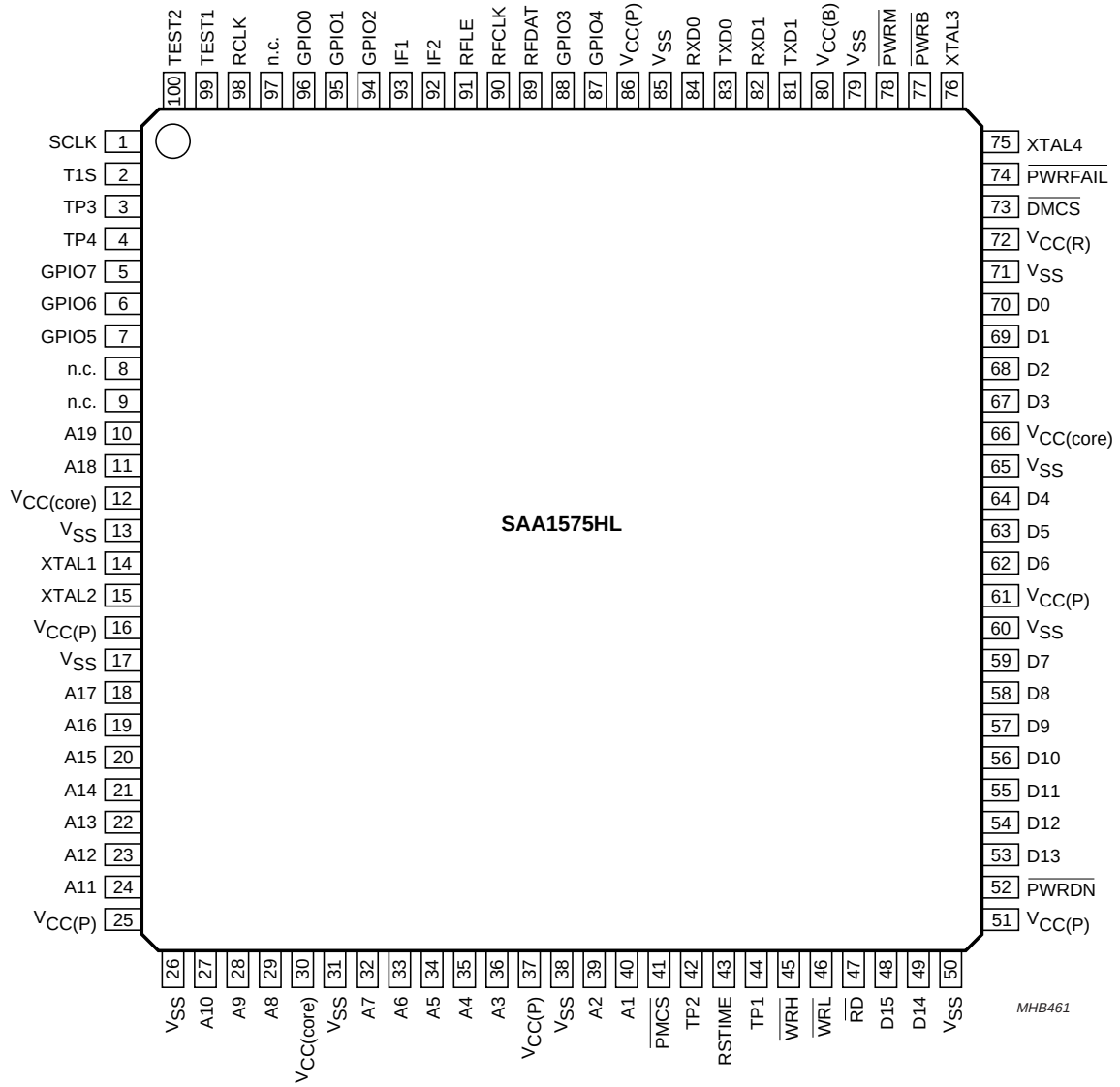


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Overview

The function of the SAA1575HL is to accept any IF data (1 or 2-bit) from a front-end RF IC (such as the UAA1570HL) and provide a serial NMEA compatible GPS position and time output. The IF input is sampled synchronously with the front-end reference clock, SCLK. Data is decoded from the IF input stream by one of eight parallel correlators which allow up to eight satellites to be tracked at one time. The acquisition, allocation and tracking of the satellites is performed under firmware control by the on-chip processor.

In addition to the SAA1575HL and an appropriate front-end IC (such as the UAA1570HL), the only external components required to complete a functional GPS receiver are some RAM, the firmware ROM and some discrete devices to control the power supplies. The need for external glue logic is eliminated by various chip-select functions implemented on the SAA1575HL.
The SAA1575HL also contains an optional independent Real-Time Clock (RTC) which requires a separate 32.768 kHz crystal. This can be set to GPS time by the processor and enables fast re-acquisition (a warm start) of satellites after power has been switched off. A separate supply pin is provided to allow the RTC to be powered while the rest of the IC is turned off.

The block diagram of the SAA1575HL is shown in Fig.1. The IC consists of a processor core, its associated peripherals, some internal memory and a series of GPS correlators.

The processor core is based on an embedded Philips 80C51XA (known as the XA). The XA peripherals (UARTs, timers, watchdog and general purpose I/Os) are termed special function registers and are memory mapped in parallel with an area of the data memory. They are connected to the core by dedicated data and address buses. The internal data memory is also connected to the core by a dedicated bus.

The rest of the IC (the correlators, RTC and system control) is mapped into the external data memory space. The multiplexed data and address buses provided by the XA core are separated by an on-chip latch to provide the distinct 16-bit data bus and 19-bit address bus. These are made available externally for connection to external memory via the external bus interface.

The correlators, RTC and system control blocks are memory mapped into the highest page of the 16 pages in the XA data structure.

Both the RTC and the correlators are asynchronous to the system clock, with synchronization being achieved by firmware and interrupts.

7.2 The 80C51XA processor

The microcontroller core in the SAA1575HL is a Philips design called the XA (eXtended Architecture) which is an extended 80C51-like 16-bit microcontroller. This is largely compatible with the 8051 but with various improvements. The main features of the XA compared to the 8051 can be summarized as follows:

- 16-bit versus 8-bit data processing
- 20-bit versus 16-bit address bus
- 3 clock instruction cycle versus 12 clock instruction cycle
- 10 Mips versus 1 Mips
- 20 CPU registers versus 1 accumulator
- All 20 CPU registers in the XA can be used as the accumulator register in the 8051
- 16×16 multiplication in 12 clocks, $^{32}/_{16}$ division in 22 clocks
- New type of instructions such as normalization, sign extension and trap
- Multi-tasking support versus no multi-tasking support.

7.3 The GPS correlators

The correlator block forms the GPS specific hardware for correlating with the direct sequence spread spectrum GPS signals. The 8 identical correlators share the 2-bit IF input and the sample clock of the Analog-to-Digital Converter (ADC) of the front-end. The input signal is the 50 bits/s GPS data spread by the 1.023 Mbits/s PN code and modulated by the residual carrier. The residual carrier frequency is composed of the Doppler frequency and the receiver local oscillator frequency offset.

To recover the GPS data and find the accurate timing of the received data for GPS navigation from the low-level (as low as −130 dBm) GPS signal, the residual carrier frequency and phase have to be found by a Phase-Locked Loop (PLL) with minimum tracking phase error.
The starting position of the PN code in the received signal is found by correlation within a Delay-Locked Loop (DLL). The channel correlator includes a local numerically controlled oscillator and a programmable local PN code generator with the phase rotation and correlation circuit.

7.4 Memory organization

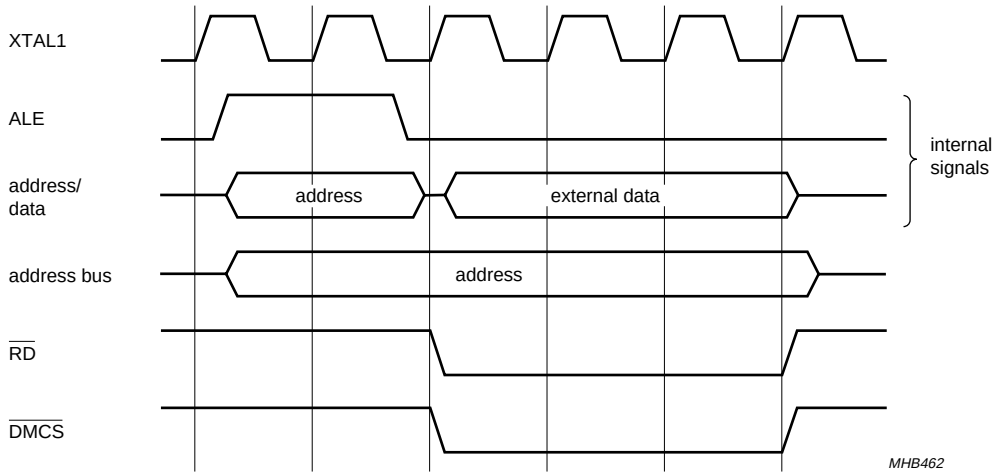
The memory space in the SAA1575HL is configured in a Harvard architecture which means that the code and data memory are organized in separate address spaces. This section describes the SAA1575HL memory requirements.

7.4.1 DATA MEMORY SPACE

The SAA1575HL contains 2 kbytes words of internal data memory. For correct firmware operation, a further 32 kbytes words of external data memory is needed with a maximum access time of 100 ns.

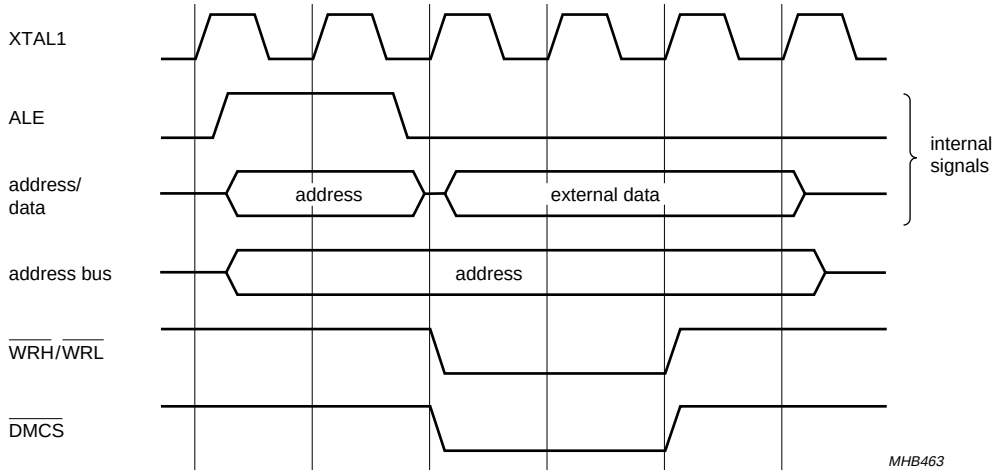
The specifications of this external memory are firmware dependent. The figures given in this document are for the standard Philips firmware. With other revisions of firmware the timings could differ by integer numbers of XTAL1 clock cycles.

In the SAA1575HL, all of the data read and write cycles are preceded by an internal Arithmetic and Logic Elements (ALEs) cycle (as in any standard 80C51 system).
The multiplexed address/data bus and the ALE signal are not available externally. However, for clarity, these are illustrated in Figs 3 to 6.



The timing is configurable under firmware control.

Fig.3 Example of external data read (standard firmware).



The timing is configurable under firmware control.

Fig.4 Example of external data write (standard firmware).

7.4.2 CODE MEMORY SPACE

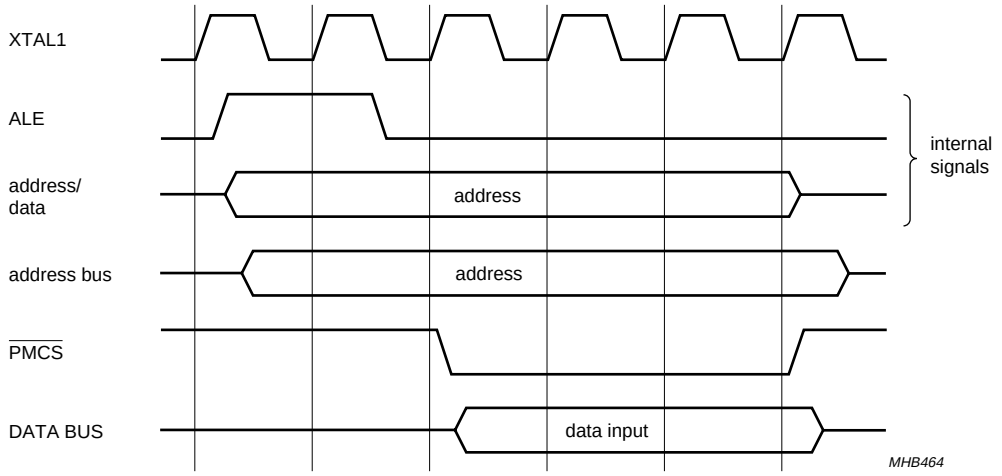
The SAA1575HL has no internal code memory. The GPS solution firmware resides in external memory. With the standard Philips firmware, a ROM with a maximum access time of 100 ns is required.

The classic operation of a multiplexed address/data bus involves an address being set-up for every bus cycle. The internal ALE signal is used to latch the address prior to the cycle on which the data is set-up. An example of the resulting timing is illustrated in Fig.5.

The SAA1575HL does not require an internal ALE cycle for each code fetch. The lowest 3 address lines are not multiplexed with the data lines and so these can be used to incrementally read code locations.

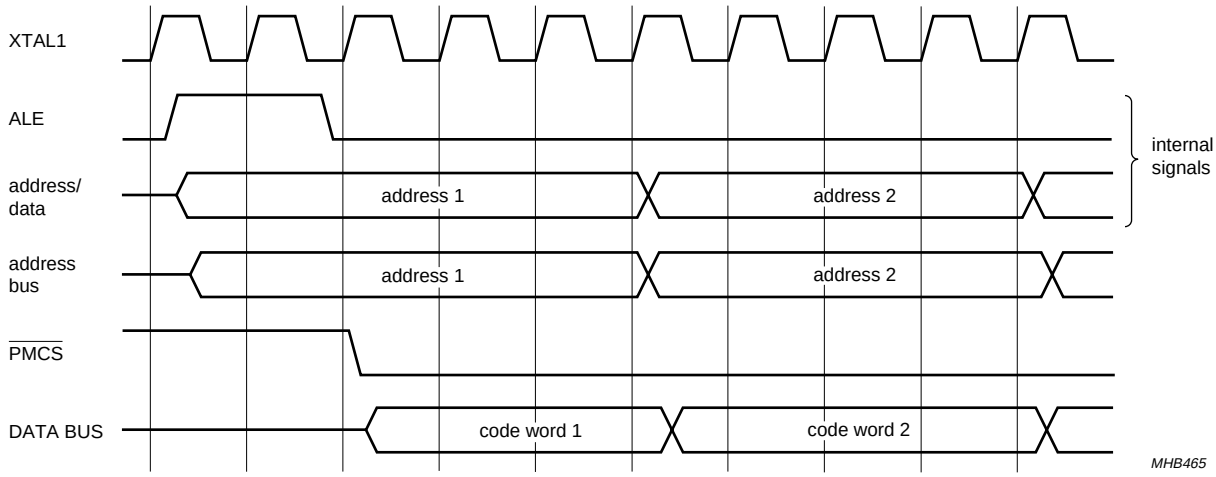
The XA core can therefore issue up to 8 word reads through sequential code memory for each ALE cycle. This is termed a burst code read. An example of the resulting timing is illustrated in Fig.6.

Any type of branch or jump in the program may require a code fetch in a non-sequential manner and a new ALE cycle will be needed. This may occur at any stage in a code read. Thus the length of the read strobe in a burst read is not necessarily an integer multiple of the individual code read length.



The timing is configurable under firmware control.

Fig.5 Example of code read with ALE (standard firmware).



The timing is configurable under firmware control.

Fig.6 Example of burst mode code read (standard firmware).

7.5 CPU peripheral features

The SAA1575HL contains the hardware for 3 timers, 2 UARTs, a watchdog timer, a 3-bit RF IC programming link and an 8-bit general purpose I/O port.

7.5.1 TIMERS/COUNTERS

The SAA1575HL has 2 standard 16-bit timer/counters and a third 16-bit up/down timer/counter. These timer/event counters can perform the following functions:

- Measure time intervals and pulse duration
- Count external interrupts
- Generate interrupt requests
- Generate Pulse Width Modulation (PWM) or timed output waveforms.

The timers are used by the standard Philips firmware to generate the baud rates for the UART serial ports. The additional features are not used in the standard Philips firmware but are available for use in custom firmware revisions.

All of the timers are configured in the 16-bit auto-reload mode of operation. Timer 1 is used to generate the baud rate for UART0 and Timer 2 is used to generate the baud rate for UART1. In the standard Philips firmware, Timer 0 is not used.

7.5.2 WATCHDOG TIMER

The watchdog timer protects the system from incorrect code execution by causing a processor reset if the watchdog timer underflows as a result of a failure of the firmware to feed the timer prior to it reaching its terminal count.

In the standard Philips firmware, the watchdog is enabled with a time-out period of 130 ms (at a clock frequency of 30 MHz).

7.5.3 UARTS

The SAA1575HL contains 2 UART ports, compatible with the enhanced UART modes 1 to 3 on the 8xC51FB (mode 0 operations not supported). With the exception of the removal of the mode 0 operation, the UARTs in the SAA1575HL are identical to those in the XA-G3 product. Each UART rate is determined by either a fixed division of the oscillator (in UART mode 2) or by one of the timer overflow rates (in UART modes 1 and 3).

With the standard Philips firmware, both UARTs are configured to be in Mode 1: variable rate 8-bit operation. Ten bits are transmitted (via TXDn) or received (via RXDn): a START bit, 8 data bits (LSB first), and a STOP bit.

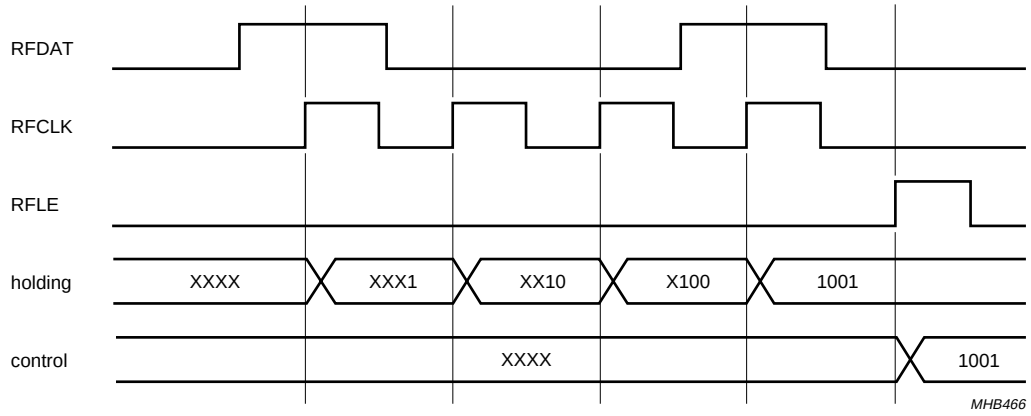
In general, the UART clocks (which are 16 times the baud rate) are determined by the Timer 1 or Timer 2 overflow rate. With the standard Philips firmware, Timer 1 is used to generate the baud rate for UART0 and Timer 2 is used to generate the baud rate for UART1. The baud rate is set to be 4800 bits/s for both UARTs.

7.5.4 RF IC PROGRAMMING PORT

The SAA1575HL is capable of programming the UAA1570HL via a standard 3-wire serial link. This consists of a clock line (SCLK), data line (D15 to D0) and a latch enable (RFLE). Data is clocked into a holding register in the UAA1570HL serially on each rising edge of the output RFCLK. Once the complete serial packet has been clocked into the RF IC, the latch enable output, RFLE, is asserted which copies the new word from the holding register in the RF IC into the control registers.

Proper timing of the clock, data and latch outputs is ensured by firmware. An example sequence is illustrated in Fig.7. The signals shown would result in the value 1001 being loaded into the last 4 bits of the RF IC serial register. Each loading operation of the RF IC reloads the complete RF control register.

With the standard Philips firmware, a 20-bit long word 0X5E320 is transmitted in this manner on start-up or re-initialization. This gives full compatibility with the Philips UAA1570HL front-end IC. See the *"UAA1570HL"* for more details about the configuration options of the front-end IC.



X = don't care.

Fig.7 Example timing for UAA1570HL programming.

7.5.5 General purpose I/O

The SAA1575HL possesses an 8-bit general purpose I/O register and 8 associated I/Os (see Fig.8). With the standard Philips firmware, all 8 of these pins are configured as outputs.

With the standard Philips firmware, only pin GPIO0 is used. This is switched on at the end of the firmware initialization sequence and remains on subsequently.

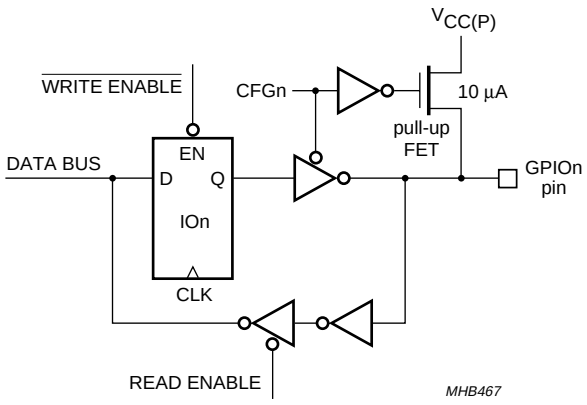


Fig.8 GPIO pin drive circuits.

7.6 The real-time clock

The Real-Time Clock (RTC) is a functional unit used to generate time information. Its purpose is to supply approximate GPS time to the system firmware for the initial acquisition of satellites (a warm start). The power supply for the RTC is separate from the rest of the IC, allowing a low capacity battery to be used to maintain the low power RTC function.

The timebase for the RTC should be provided by a dedicated 32.768 kHz crystal which can be omitted if the RTC is not required. This is divided down by a fixed divider to provide the 1 Hz timebase used for the rest of the RTC block. A digital sampling circuit is also included to prevent digital noise due to the on-chip processor causing incorrect timekeeping.

The SAA1575HL uses a digital under-sampling system to ensure that ground bounce does not cause RTC timekeeping errors. This places a restriction on the ratio of XTAL1 and XTAL3 frequencies for which the RTC will operate correctly. This has been optimistic for the case f_{XTAL1} = 30 MHz, f_{XTAL3} = 32 kHz and, assuming that the RTC crystal frequency will always be 32 kHz, will operate correctly for the entire specified range of system frequencies.

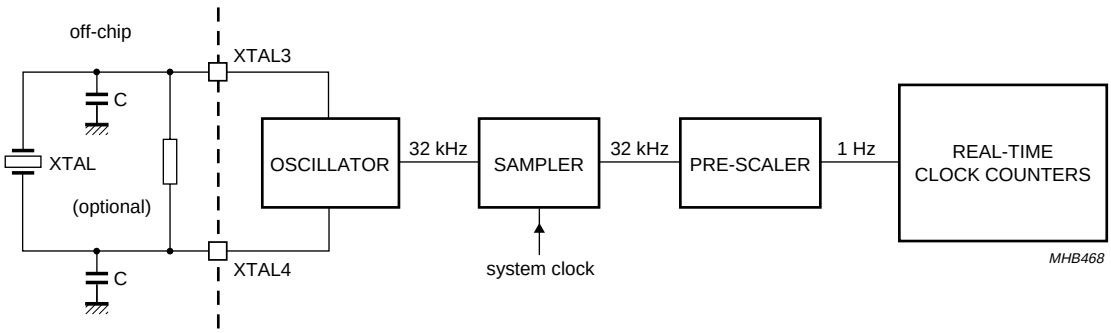


Fig.9 Real-time clock circuit.

7.7 The external bus

The off-chip memories and the on-chip registers are on the same address and data bus. The routing of the data and address signals between the on-chip registers and the off-chip memories is controlled by a block known as the external bus interface. In addition, certain chip enable signals are decoded within the block to reduce the amount of external glue logic required in the complete system.

The address latch, normally required on 80C51 systems, is implemented within the SAA1575HL. Therefore, no ALE signal is seen outside the IC and address and data lines are brought out on separate pins.

However, since internally there is still the need to latch the address from a common address/data bus, signals on the data bus will be seen to change during the address set-up cycles.

The lower 3 external address lines are driven directly by the XA core and are not latched. This allows ‘burst’ code reads to be performed in which adjacent code locations are accessed without the need for an address latch cycle.

Signals similar to those used by a standard 80C51 or XA system are used to control the external bus activity.

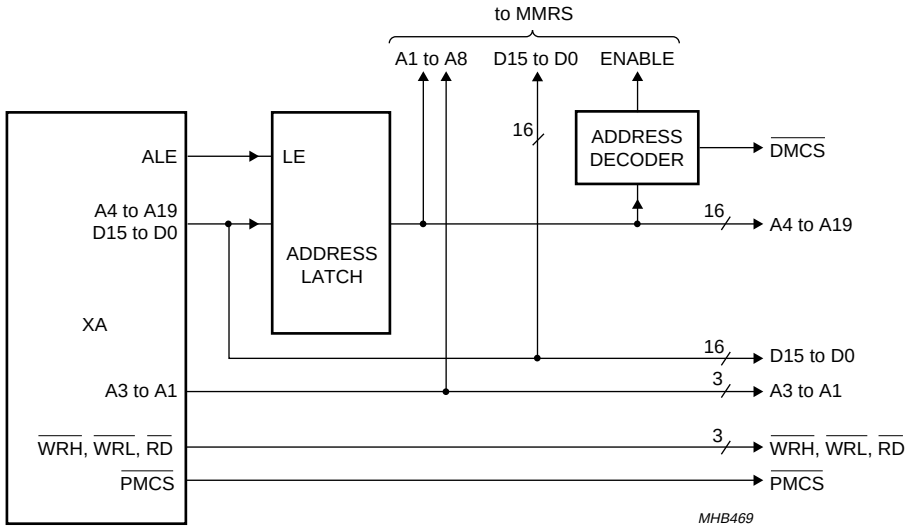


Fig.10 SAA1575HL internal address and data routing.

7.7.1 PROGRAM MEMORY CHIP SELECT

This signal ($\overline{PMCS}$) is an active LOW strobe used to enable the output of the external code memory. It remains HIGH when a read code is not in progress.

7.7.2 DATA MEMORY CHIP SELECT

This signal ($\overline{DMCS}$) is an active LOW strobe used to enable the external data memory. The SAA1575HL hardware supports two distinct modes of operation of this signal (selected in firmware) designed for optimum power or optimum speed. The standard Philips firmware is configured for optimum power.

$\overline{DMCS}$ is taken LOW during an external data read or write operation to segments 0 to 14 of the memory map. To prevent the corruption of external data memory, the $\overline{DMCS}$ pin is driven on the backup supply voltage and will be held HIGH once the $\overline{PWRFAIL}$ signal has been asserted LOW.

With the standard Philips firmware, the $\overline{DMCS}$ signal is gated by the external access read and write strobes. This should significantly reduce the power consumption of the external RAM but may require the use of a slightly faster external memory (depending on clock speed and details of the external memory used).

7.7.3 READ STROBE

This signal ($\overline{RD}$) is an active LOW strobe used to indicate that the XA is expecting data from the external bus.

7.7.4 WRITE LOW BYTE STROBE

This signal ($\overline{WRL}$) is an active LOW strobe used to indicate that the XA is performing an external write. This strobe only applies to the lower data byte of the 16-bit data word, allowing byte writes to be performed from the 16-bit data. This strobe will also be taken LOW for word write operations.

7.7.5 WRITE HIGH BYTE STROBE

This signal ($\overline{WRH}$) is an active LOW strobe used to indicate that the XA is performing an external write. This strobe only applies to the higher data byte of the 16-bit data word, allowing byte writes to be performed from the 16-bit data. This strobe will also be taken LOW for word write operations.

7.8 Backup supplies and reset

The SAA1575HL is designed to operate correctly in situations when the main power supply fails. In addition to the main core and peripheral power supplies, separate pins are provided for backup core and peripheral supplies which enable critical (and low-power) functions to be maintained during the loss of main power. There is also an on-chip reset timer which will aid the design of a full power-down strategy.

7.8.1 SUPPLY DOMAINS

To allow for the use of inexpensive 5 V external components, the periphery of the SAA1575HL can be powered with a higher voltage than the core. Therefore there is a distinction between the core and peripheral power supplies. In addition, there is the need to maintain certain functionality on a low-power supply in the event of main power failure. Therefore there are 2 additional supplies required for so-called backup operation. Thus there are four distinct power supply domains, two for the core supplies and two for the peripheral supplies.

Table 1 Supply domains

SUPPLY	DESCRIPTION	PURPOSE
$V_{CC(core)}$	main core supply (3 V)	provides power for all core circuits, excluding those mentioned below
$V_{CC(P)}$	main peripheral supply (3 to 5 V)	provides power for all pins, excluding those mentioned below
$V_{CC(R)}$	RTC core supply (2.4 to 3 V)	powers the real-time clock, the 32 kHz oscillator and the 32 kHz de-bounce circuit; it also produces the signals for $\overline{DMCS}$, $\overline{PWRM}$ and $\overline{PWRB}$
$V_{CC(B)}$	backup peripheral supply (2.4 to 5 V)	provides power for the following pins: $\overline{DMCS}$, $\overline{PWRM}$, $\overline{PWRB}$ and $\overline{PWRFAIL}$

In normal operation, the backup core and pad supplies should be provided from the main power supply rather than a low-capacity battery since the power drawn on the backup supplies while the processor is operating may be significant. Two output pins, $\overline{PWRM}$ and $\overline{PWRB}$ are provided to control this switching.

The power consumption of the SAA1575HL in the power-down mode is minimal since no outputs are changing. The only active circuit in power-down is the real-time clock.

Isolation between the power domains is controlled by the $\overline{\text{PWRFAIL}}$ input pin. This must be driven LOW in a power-failure situation to ensure that the backup domains are isolated from the main supply domains. If this is not done, it is possible that the registers contained in the backup supply domain will be corrupted as the main supply is cycled. It is also possible that under these circumstances a high backup supply current will be drawn (depending on details of the external supply circuitry).

7.8.2 Power-down design strategy

In power-down operation the main supplies are assumed to have failed. The backup core and pad supplies should be switched to backup power. The detection of the power failure and the power supply switching is the responsibility of the user. However, the SAA1575HL does provide several functions to aid this task.

The power-down and power-fail operations of the SAA1575HL are controlled by two inputs, $\overline{\text{PWRDN}}$ and $\overline{\text{PWRFAIL}}$, which are assumed to be connected to external voltage comparators. The use of external comparators allows the voltage thresholds to be set by the system designer. It also allows a certain amount of flexibility as to which supplies are monitored for power failure.

7.8.2.1 Power-down control signals

The power-down control signal pins (see Table 2) are either inputs or outputs associated with the SAA1575HL power control. The descriptions are for the intended use of the control signals in a normal application.

For a correct reset to occur, it is important that $\overline{\text{PWRFAIL}}$ should be held LOW as long as minimum voltages have been established on all four of the power supply domains. If this is not done various serious consequences may occur, including main oscillator failure, a high supply current state, a processor crash or RTC register corruption.

Table 2 Power-down control signals

SIGNAL	FUNCTION
$\overline{\text{PWRDN}}$	**Power-down indicator**: this should be driven LOW by an external comparator to indicate impending power failure. Internally it sends an interrupt to the processor used to initiate a power-fail routine. At the end of this routine the standard firmware forces the processor into reset. This also inhibits the external RAM chip select. Reset is only de-asserted a set time after both $\overline{\text{PWRDN}}$ and $\overline{\text{PWRFAIL}}$ go HIGH, controlled by the RSTIME input.
$\overline{\text{PWRFAIL}}$	**Power fail indicator**: this should be driven LOW by an external comparator to indicate immediate power failure. Internally it forces immediate reset of the processor, isolation of the RTC and inhibition of the external RAM chip select. It also controls the power switch outputs $\overline{\text{PWRB}}$ and $\overline{\text{PWRM}}$. Reset is only de-asserted a set time after both go HIGH, controlled by the RSTIME input.
RSTIME	**Reset timer control**: this sets the time delay between de-assertion of both $\overline{\text{PWRDN}}$ and $\overline{\text{PWRFAIL}}$ and the de-assertion of the processor reset. If HIGH, the delay is approximately 10 ms. If LOW the delay is approximately 10 μs.
$\overline{\text{DMCS}}$	**External RAM chip select**: this is driven via the backup supplied core and pads. In power-down this is isolated from the rest of the IC and the output held HIGH to prevent corruption of the external RAM.
$\overline{\text{PWRM}}$	**Main power supply control**: in normal operation this is held LOW. This can be used to switch the main supplies to all of the supply input pins. In normal operation the backup pad supply pin should be driven by the main supply and the backup core supply pins should be driven by the main core supply. When the IC goes into power-down mode this output goes HIGH. In power-down the backup supply pins should be driven by their appropriate supplies.
$\overline{\text{PWRB}}$	**Backup power supply control**: this is the inverse of $\overline{\text{PWRM}}$

7.8.2.2 Example of strategy for slow supplies

The ultimate use of the power control signals is up to the user. However, two possibilities are presented as design examples. The first example will operate correctly in circuits where the rise times of the power supplies is slow compared to any delay between the supplies to the peripheral and core power domains.

In this example, both the $\overline{\text{PWRDN}}$ and $\overline{\text{PWRFAIL}}$ logic inputs to the SAA1575HL are derived by comparing the $V_{CC(P)}$ supply voltage against known references.
In general, since it is a lower voltage, the $V_{CC(core)}$ supply may hold and reach it's nominal voltage quicker than the $V_{CC(P)}$ supply.

As $V_{CC(P)}$ falls, the first threshold is reached and $\overline{\text{PWRDN}}$ is taken LOW. This triggers an interrupt in the firmware which is used to perform any required housekeeping. It is assumed that there is time for this to be completed before complete supply failure.

At the end of the interrupt routine, the firmware places the SAA1575HL into reset. As $V_{CC(P)}$ continues to fall, the second threshold is reached and is taken LOW. This toggles the power controls, both $\overline{\text{PWRM}}$ and $\overline{\text{PWRB}}$, and will force a reset if it has not already occurred.

On power-up, the power controls both $\overline{\text{PWRM}}$ and $\overline{\text{PWRB}}$ will be switched once the second threshold voltage is reached. As the supply voltage rises further, the first voltage threshold will be reached at which time both $\overline{\text{PWRDN}}$ and $\overline{\text{PWRFAIL}}$ will be HIGH. This starts the reset counter and the SAA1575HL will remain in reset until a set time after this, depending on the state of the input pin RSTIME.

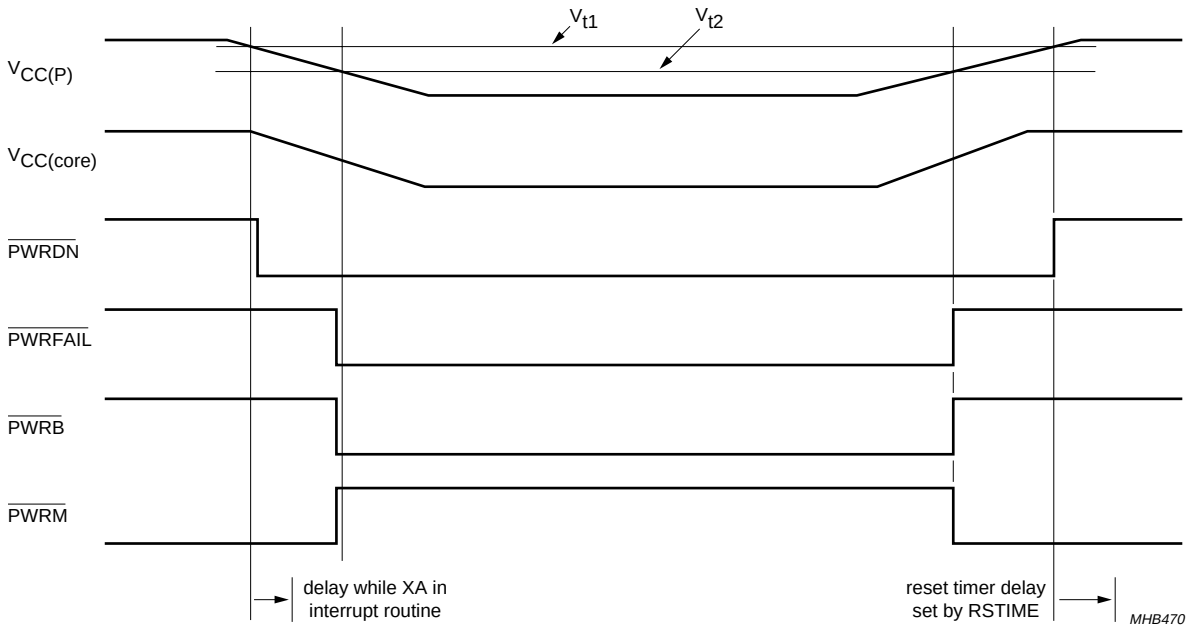


Fig.11 Example of power-down strategy with slow supplies.

7.8.2.3 Example of strategy for fast supplies

The second example will operate correctly in circuits where the delay between the supplies to the peripheral and core power domains is significant compared to the rise times of the power supplies. This may occur in cases where the core supply is a regulated (delayed) version of the peripheral supply. If the previous strategy were used in this situation, it would be possible for the SAA1575HL to miss the $\overline{\text{PWRFAIL}}$ LOW state at power-up, resulting in the IC not being given a correct reset.

In this example, the $\overline{\text{PWRDN}}$ logic input is derived as before by comparing the $V_{CC(P)}$ supply voltage against a known reference voltage. But in this instance the $\overline{\text{PWRFAIL}}$ logic input is derived by comparing the $V_{CC(core)}$ core supply against a threshold voltage.

As $V_{CC(P)}$ falls, the first threshold level is reached and $\overline{\text{PWRDN}}$ is taken LOW. This triggers an interrupt in the firmware which is used to perform any required housekeeping. At the end of the interrupt routine, the firmware places the SAA1575HL into reset.

However, if the fall times on the supplies is fast, it is likely that the $\overline{\text{PWRFAIL}}$ input will go LOW before the interrupt routine has been completed. This would force the SAA1575HL into immediate reset. At this time both $\overline{\text{PWRM}}$ and $\overline{\text{PWRB}}$ toggle to switch backup supply sources.

On power-up, the $V_{CC(P)}$ supply rises quickly. However, since this only controls an interrupt flag and the SAA1575HL is still held in reset by $\overline{\text{PWRFAIL}}$, this has no effect. Only once the $V_{CC(core)}$ supply rises will $\overline{\text{PWRFAIL}}$ be de-asserted. This can only occur once the $V_{CC(core)}$ voltage has reached the set threshold, and so there is no risk of the IC 'missing' the reset pulse. The SAA1575HL will come out of reset a set time after this, depending on the state of the input pin RSTIME.

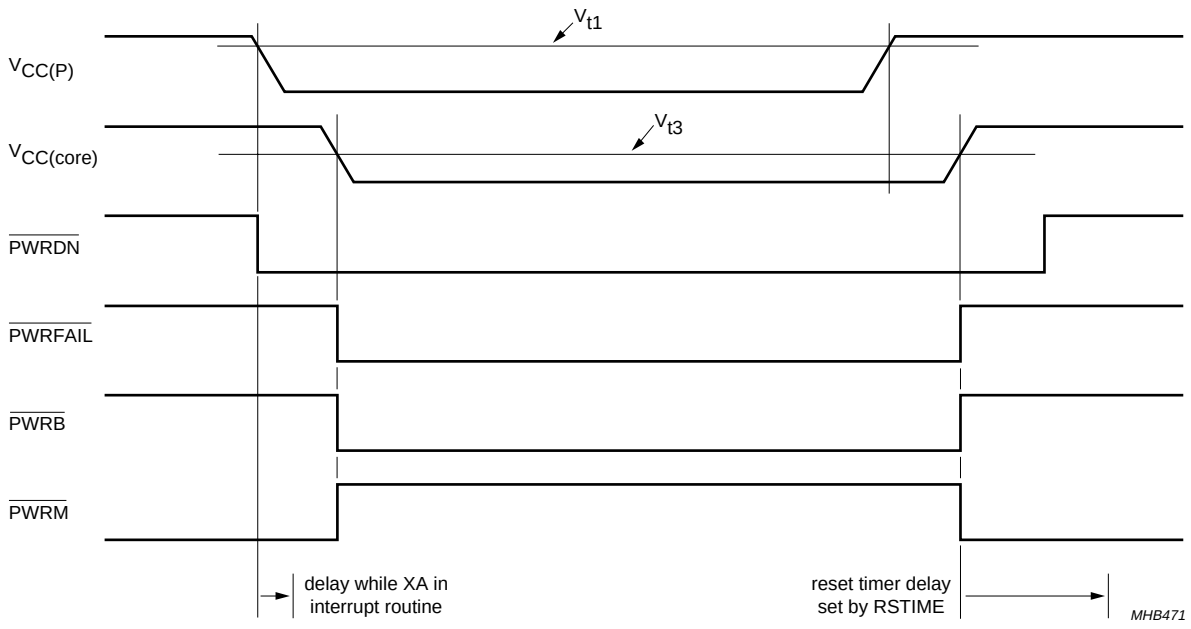


Fig.12 Example of power-down strategy with fast supplies.

7.8.3 System reset control

The SAA1575HL contains an internal timer and control logic to perform various system reset tasks. Control of this logic is by three external pins, $\overline{\text{PWRDN}}$, $\overline{\text{PWRFAIL}}$, and RSTIME. This allows the system designer to set the voltage thresholds at which the system goes into and comes out of reset.

7.8.3.1 The reset timer

The heart of the reset system is a 20-bit counter with asynchronous reset, clocked from the XTAL1 system clock. The reset counter is asynchronously reset if the $\overline{\text{PWRFAIL}}$ pin is LOW. Once reset, the counter will only be enabled once both $\overline{\text{PWRFAIL}}$ and $\overline{\text{PWRDN}}$ go HIGH. This prevents the SAA1575HL from leaving the reset state until both power detect inputs have flagged the power system as healthy.

The internal reset signal is generated by decoding the reset counter. The decode value, and hence the time delay, is controlled by the reset time control pin, RSTIME.

Table 3 Reset time control

RSTIME INPUT	NUMBER OF CYCLES BEFORE RESET DE-ASSERTED	TIME DELAY (f_{XTAL1} = 30 MHz)
1	294 912	9.8 ms
0	288	9.6 μs

The internal reset is de-asserted a given number of XTAL1 clock cycles after $\overline{\text{PWRFAIL}}$ and $\overline{\text{PWRDOWN}}$ go HIGH. It is suggested that for most applications RSTIME should be held HIGH, giving a reset time of approximately 10 ms. This would be needed to allow the on-chip oscillator to stabilize after power-up. The shorter reset time can be used for applications using an external XTAL1 clock signal which does not need a long stabilization period.

It is important that $\overline{\text{PWRFAIL}}$ should be LOW during power-up of the IC to give the correct reset.

7.8.3.2 Overall reset operation

The assertion of the reset signal (by means already described) will cause the following to occur:

- Internal XA processor reset
- Internal registers reset
- Data bus pins set to be inputs
- Read and write strobes de-asserted
- GPIO pins set to be inputs
- On-chip XTAL1 oscillator enabled.

7.8.3.3 CPU reset operation

Assuming that the correct external $\overline{\text{PWRFAIL}}$ sequence is generated on power-up, the internal XA will receive the correct reset signal from the on-chip reset block. If the proper $\overline{\text{PWRFAIL}}$ is not performed, the operation of the on-chip reset block cannot be guaranteed and the XA may fail wholly or in part.

The embedded XA requires a minimum length of reset to complete the various tasks. This minimum length is guaranteed by the on-chip reset block. The only restriction on the length of the pulse is that is should be long enough to be asynchronously detected by the SAA1575HL (typically 10 ns).

The embedded CPU can also be reset by the watchdog timer (this may be disabled on some custom firmware revisions).

7.8.4 Power saving modes

The SAA1575HL supports two power saving modes; Idle mode and sleep mode. Both modes are selected by firmware (or message over the serial link if included in the firmware). In addition, the input to any of the correlators can be inhibited individually (by firmware) which will reduce the power consumed by the block to only the clock tree dissipation.

7.8.4.1 Sleep mode

The sleep mode is intended to overlay the function of the standard 80C51XA Idle mode. Sleep is initiated by a firmware or external serial link command. This initiates a firmware routine which performs the following:

1. Send serial command to power-down RF IC (UAA1570HL)
2. Inhibit RCLK, IF2 and IF1 inputs to SAA1575HL
3. Enter standard 80C51XA Idle state.

In sleep mode the RCLK and IF inputs are prevented from entering the IC. This capability is included to cover the situation in which the SAA1575HL is used with a front-end which does not respond to the power-down command in a similar way to the UAA1570HL. Sleep mode can be exited by any active hardware interrupt, for example a UART interrupt. The sleep mode has no effect on the operation of the RTC.

7.8.4.2 Idle mode

The Idle mode is initiated by a firmware or external serial link command. This is a direct use of the standard 80C51XA Idle mode. The interrupt signals from the active peripherals such as UARTs, timers, host interface and external interrupts will cause the CPU to resume execution from the point at which it was halted. In the Idle mode, all of the output pins retain their logic states from their 'pre-idle' position. No other action is taken on entering Idle mode. In particular, the correlators will remain active since RCLK, IF1 and IF2 will not be prevented from entering the IC.

7.9 Clock signals and oscillators

The SAA1575HL requires 3 clock signals for full operation:

- XTAL1: Processor (system) clock
- XTAL3: Real-time clock crystal frequency (optional)
- RCLK: GPS reference clock.

Two of these clocks, XTAL1 and XTAL3, can be generated by on-chip oscillator circuits. The third, RCLK, must be supplied from an external source; in most applications a temperature compensated oscillator module.

7.9.1 SYSTEM CLOCK (XTAL1)

The SAA1575HL requires a system clock for the on-chip processor and related peripheral blocks. This can be provided from an external clock source via the XTAL1 input pin or by using the on-chip oscillator circuit with an external resonating element connected between the XTAL1 and XTAL2 pins. In most circumstances this would be an external crystal accompanied by two capacitors connected to ground, a series resistor (to optimize power consumption) and a shunt resistor to ensure start-up under all conditions.

Optimum values of C, R_P and R_S will depend on the crystal used. However, typical values would be C = 20 pF, R_P = 1 MΩ and R_S = 200 Ω. The hardware places a restriction on the range of frequencies for which correct operation will occur; 26 MHz < f_{XTAL1} < 32 MHz.

However, the restriction on operating frequency imposed by the firmware is tighter than this. The standard Philips firmware has been written on the assumption of a 30 MHz system clock frequency.

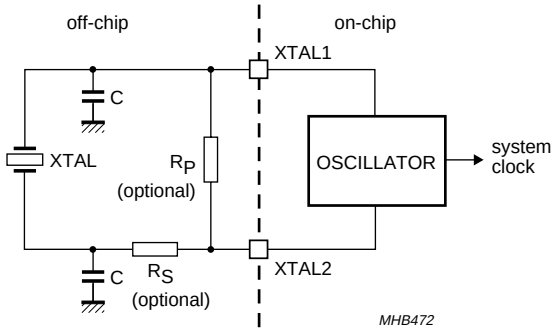


Fig.13 System clock oscillator circuit.

7.9.2 RTC CLOCK (XTAL3)

If the on-chip real-time clock is required (as with the standard Philips firmware), a low frequency clock signal is required to run the clock. The SAA1575HL is designed so that a standard 32.768 kHz watch crystal can be used for this purpose. Since this is much slower than the system clock, a much lower power is required to run just the real-time clock, allowing it to be powered from a low-capacity battery when the main power supply fails.

As with the system clock, there is an on-chip oscillator so that only a few passive external components are required. These would be an external crystal accompanied by two capacitors connected to ground, a series resistor (optional) and a shunt resistor to ensure start-up under all conditions.

Optimum values of C and R_P will depend on the crystal used. However, typical values would be C = 22 pF and R_P = 1 MΩ.

7.9.3 REFERENCE CLOCK (RCLK)

The reference clock input, RCLK, is used as the source for the sampling of the IF input signal. A divided-down version of RCLK is output on the sample clock pin, SCLK, for use by the front-end IC.

The division ratio of RCLK/SCLK is programmable in firmware. In the standard Philips firmware this ratio is set to 3.

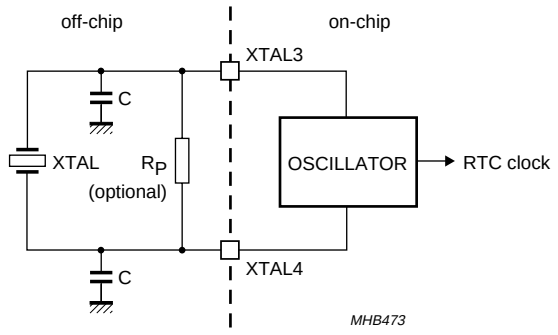


Fig.14 RTC clock oscillator circuit.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC(core)}$	core supply voltage		–0.5	+3.6	V
$V_{CC(R)}$	RTC core supply voltage		–0.5	+3.6	V
$V_{CC(P)}$	peripheral DC supply voltage		–0.5	+5.5	V
$V_{CC(B)}$	backup peripheral DC supply voltage		–0.5	+5.5	V
ΔV_{CC}	absolute voltage differences between two V_{CC} pins		–	550	mV
P_{tot}	total power dissipation		–	500	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	ambient temperature	$V_{CC(core)} = V_{CC(R)} = 3.3$ V; $V_{CC(P)} = V_{CC(B)} = 5.0$ V	–40	+85	°C
V_{es}	electrostatic handling	note 1	2000	–	V
		note 2	200	–	V

Notes

1. Human body model: C = 100 pF; R = 1.5 kΩ.
2. Machine model: C = 200 pF; L = 0.75 μH; R = 0 Ω.

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	45	K/W

10 DC CHARACTERISTICS

$V_{CC(P)} = V_{CC(B)} = 5$ V; $V_{CC(core)} = V_{CC(R)} = 3$ V; $T_{amb} = 20$ °C; $f_{osc} = 30$ MHz; standard Philips firmware (release HD00); note 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{CC(core)}$	core supply voltage		2.7	3.3	3.6	V
$V_{CC(P)}$	peripheral supply voltage		2.7	5.0	5.5	V
$V_{CC(R)}$	RTC core supply voltage		2.4	3.3	3.6	V
$V_{CC(B)}$	backup peripheral supply voltage		2.7	5.0	5.5	V
$I_{CC(core)}$	core supply current	normal mode	–	35	–	mA
		idle mode	–	15	–	mA
		sleep mode	–	–	10	µA
$I_{CC(P)}$	peripheral supply current	normal mode; note 2	–	20	–	mA
		idle mode	–	–	1	mA
		sleep mode	–	–	1	mA
$I_{CC(R)}$	RTC core supply current	normal mode; note 3	–	10	30	µA
		idle mode; note 3	–	10	30	µA
		sleep mode; note 3	–	10	30	µA
$I_{CC(B)}$	backup peripheral supply current	normal mode; note 2	–	5	–	mA
		idle mode	–	1	–	µA
		sleep mode	–	1	–	µA
Inputs: pins $\overline{\text{PWRFAIL}}$, $\overline{\text{PWRDN}}$, RSTIME, RXD1, RXD0, IF2, IF1, RCLK, TEST1, TP1, TP2, TP3 and TP4						
V_{IL}	LOW-level input voltage		–	–	1.5	V
V_{IH}	HIGH-level input voltage		3.5	–	–	V
Outputs (LOW drive current): pins $\overline{\text{PWRB}}$, $\overline{\text{PWRM}}$, T1S, RFCLK, RFDAT, RFLE and TEST2						
V_{OL}	LOW-level output voltage	$I_{OL} = 2.0$ mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	$I_{OH} = 0.5$ mA	2.4	–	–	V
$I_{drive(max)}$	maximum drive current		–	–	2	mA
$C_{L(max)}$	maximum load capacitance		–	–	50	pF
$t_{d(t)}$	transition delay	$C_L = 5$ pF	–	7.4	–	ns
		$C_L = 25$ pF	–	8.8	–	ns
Outputs (HIGH drive current): pins A19 to A1, $\overline{\text{DMCS}}$, $\overline{\text{PMCS}}$, TXD0, TXD1 and SCLK						
V_{OL}	LOW-level output voltage	$I_{OL} = 4.0$ mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	$I_{OH} = 1.0$ mA	2.4	–	–	V
$I_{drive(max)}$	maximum drive current		–	–	4	mA
$C_{L(max)}$	maximum load capacitance		–	–	100	pF
$t_{d(t)}$	transition delay	$C_L = 10$ pF	–	6.8	–	ns
		$C_L = 50$ pF	–	8.1	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I/O: pins $\overline{\text{WRL}}$, $\overline{\text{WRH}}$ and $\overline{\text{RD}}$						
V_{IL}	LOW-level input voltage		–	–	1.5	V
V_{IH}	HIGH-level input voltage		3.5	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 4.0 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 1.0 mA	2.4	–	–	V
$I_{drive(max)}$	maximum drive current		–	–	4	mA
$C_{L(max)}$	maximum load capacitance		–	–	100	pF
$t_{d(t)}$	transition delay	C_L = 10 pF	–	7.0	–	ns
		C_L = 50 pF	–	8.7	–	ns
I/O (pull-up): pins D15 to D0 and GPIO7 to GPIO0						
V_{IL}	LOW-level input voltage		–	–	1.5	V
V_{IH}	HIGH-level input voltage		3.5	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 4.0 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 1.0 mA	2.4	–	–	V
$I_{drive(max)}$	maximum drive current		–	–	4	mA
$C_{L(max)}$	maximum load capacitance		–	–	100	pF
$t_{d(t)}$	transition delay	C_L = 10 pF	–	8.9	–	ns
		C_L = 50 pF	–	11.0	–	ns
I_{pu}	pull-up current		–	10	–	µA

Notes

1. XTAL1, XTAL2, XTAL3 and XTAL4 are not specified with respect to levels.
2. Depends on all the external circuit driven by outputs.
3. Specified at RTC clock frequency of 32.768 kHz.

11 AC CHARACTERISTICS

$V_{CC(P)} = V_{CC(B)} = 5$ V; $V_{CC(core)} = V_{CC(R)} = 3$ V; $T_{amb} = 20$ °C; $f_{osc} = 30$ MHz; standard Philips firmware (release HD00); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
External clock						
f_{osc}	oscillator frequency		26	30	32	MHz
T_{clk}	clock period and CPU timing cycle		–	33.3	–	ns
t_{CLKH}	clock HIGH time	40 to 60% duty cycle	–	6.7	–	ns
t_{CLKL}	clock LOW time	40 to 60% duty cycle	–	6.7	–	ns
$t_{r(clk)}$	clock rise time		–	5	–	ns
$t_{f(clk)}$	clock fall time		–	5	–	ns
$f_{clk(ref)}$	reference clock frequency		–	14.4	35	MHz
External program memory read (non-burst code read); see Fig.16						
t_{AVAU}	address valid time period		163.7	165.7	–	ns
t_{AVPL}	address valid to $\overline{PMCS}$ asserted		62.7	65.7	–	ns
$t_{W(PMCS)}$	$\overline{PMCS}$ pulse width		97.0	98.0	–	ns
t_{PLIV}	$\overline{PMCS}$ LOW to instruction valid		–	82.0	85.0	ns
$t_{h(I)}$	instruction hold time after $\overline{PMCS}$ de-asserted		0.0	–	–	ns
t_{AVIV}	address valid to instruction valid (access time)		–	148.7	151.7	ns
$t_{su(I)}$	instruction set-up time before $\overline{PMCS}$ de-asserted		14.0	16.0	–	ns
t_{PXIZ}	bus 3-state after $\overline{PMCS}$ de-asserted		–	30.0	36.0	ns
t_h	hold time of a (3 : 1) after $\overline{PMCS}$ de-asserted		0.0	1.0	–	ns
External program memory read (burst code read); see Figs 16 and 17						
t_{AVAU}	address valid time period		131.3	132.3	–	ns
t_{AVIV}	address valid to instruction valid (access time)		–	115.3	118.3	ns
t_{IVAU}	instruction valid to address undefined		15.0	17.0	–	ns
t_{AUIU}	address valid to instruction undefined		0.0	–	–	ns
External data memory read; see Fig.18						
t_{AVAU}	address valid time period		163.7	164.7	–	ns
t_{RLEL}	$\overline{RD}$ asserted to $\overline{DMCS}$ asserted	note 1	–	2.0	4.0	ns
$t_{W(DMCS)}$	$\overline{DMCS}$ pulse width		97.0	98.0	–	ns
t_{RHEH}	$\overline{RD}$ de-asserted to $\overline{DMCS}$ de-asserted		–	2.0	6.0	ns
t_{AVRL}	address valid to $\overline{RD}$ asserted		64.7	65.7	–	ns
$t_{W(RD)}$	$\overline{RD}$ pulse width		98.0	–	–	ns
t_{AVDV}	address valid to data valid (access time)		–	148.7	151.7	ns
t_{RLDV}	$\overline{RD}$ asserted to data valid		–	82.0	85.0	ns
$t_{su(D)}$	data set-up time before $\overline{RD}$ de-asserted		15.0	16.0	–	ns
$t_{h(D)}$	data hold time after $\overline{RD}$ de-asserted		0.0	–	–	ns
t_{RHDZ}	bus 3-state after $\overline{RD}$ de-asserted		–	30.0	36.0	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
External data memory write; see Fig.19						
t_{AVAU}	address valid time		164.7	–	–	ns
t_{WLDL}	$\overline{WRH}$ and $\overline{WRL}$ asserted to $\overline{DMCS}$ asserted	note 1	–	2.0	4.0	ns
$t_{W(DMCS)}$	$\overline{DMCS}$ pulse width		65.7	–	–	ns
t_{WHDH}	$\overline{WRH}$ and $\overline{WRL}$ de-asserted to $\overline{DMCS}$ de-asserted		–	2.0	4.0	ns
t_{AVWL}	address valid to $\overline{WRH}$ and $\overline{WRL}$ asserted		63.7	–	–	ns
t_{WLWH}	$\overline{WRH}$ and $\overline{WRL}$ pulse width		64.7	65.7	–	ns
t_{AVQV}	address valid to data valid		67.7	–	–	ns
t_{QVWL}	data valid to $\overline{WRH}$ and $\overline{WRL}$ de-asserted		–9.0	–4.0	–	ns
t_{WHAU}	$\overline{WRH}$ and $\overline{WRL}$ de-asserted to address undefined		2.0	–	–	ns
$t_{h(D)}$	data hold time after $\overline{WRH}$ and $\overline{WRL}$ de-asserted		0	1.0	–	ns
GPS IF input timing; see Fig.20						
t_{FVSH}	IF set-up time before rising edge of SCLK		–	10	–	ns
t_{SHFV}	IF hold time after rising edge of SCLK		0	–	–	ns
1 second pulse output; see Fig.21						
$t_{W(T1S)}$	T1S pulse width		–	1.0	–	µs
T_{T1S}	T1S pulse period	note 2	–	1.0	–	s

Notes

1. For default $\overline{DCMS}$ operation.
2. The 1 s pulse output is only valid when at least one channel is locked.

Table 4 Explanation of symbol characters in Chapter “AC characteristics”

SYMBOL CHARACTER	DESCRIPTION
A	address
C	clock
D	input data
E	$\overline{DMCS}$ strobe
I	instruction (program memory)
P	$\overline{PCMS}$ strobe
Q	output data
R	$\overline{RD}$
W	$\overline{WRH}$ or $\overline{WRL}$ strobes
H	logic high
L	logic low
U	undefined
V	valid
Z	high impedance or pull-up

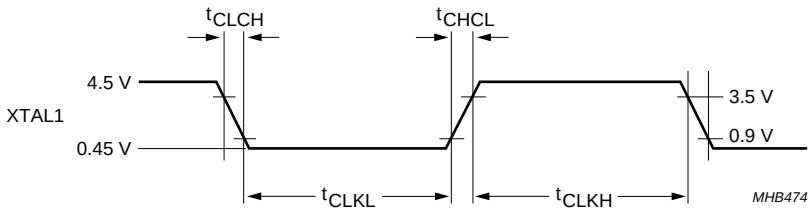


Fig.15 External XTAL1 clock drive.

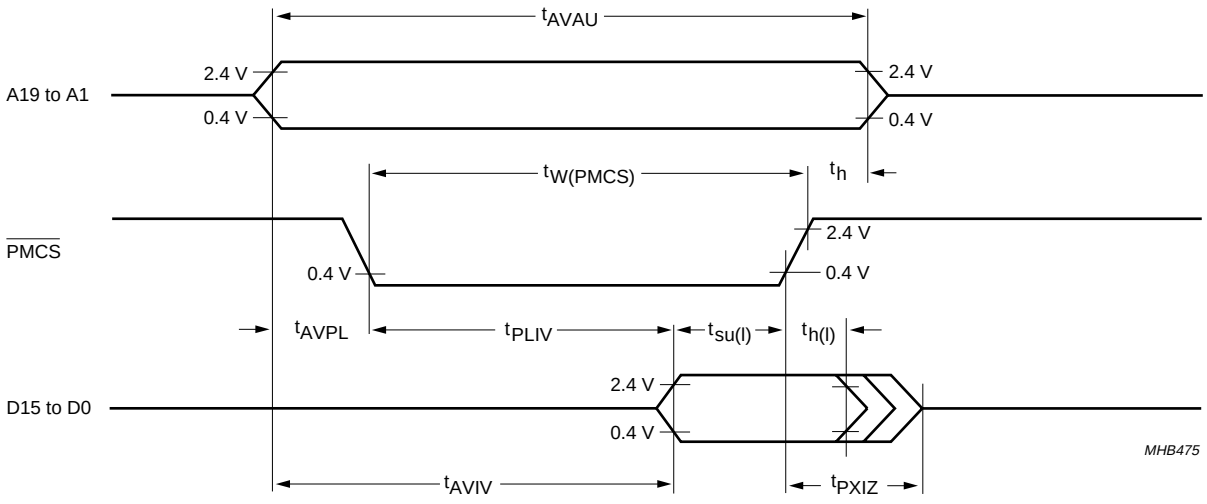


Fig.16 External program memory read cycle (non-burst).

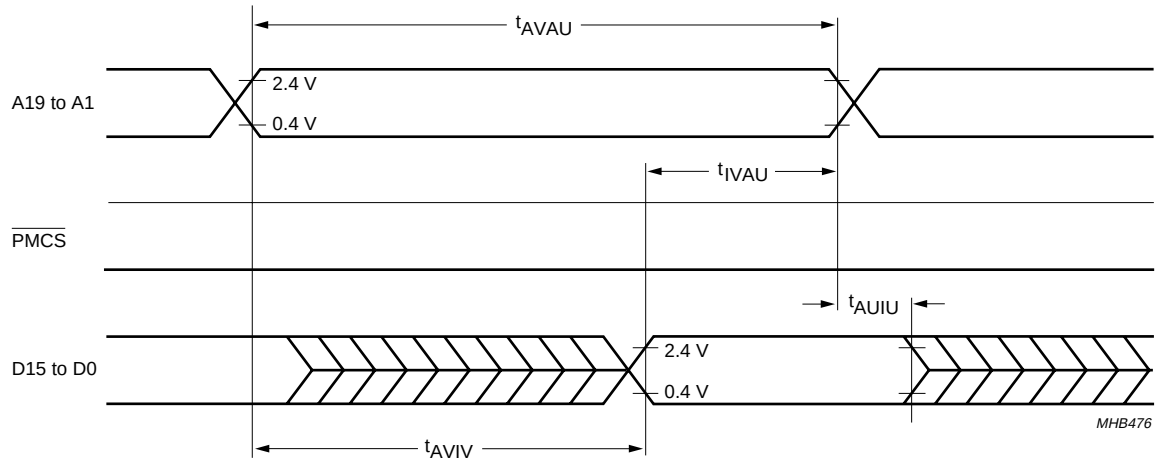
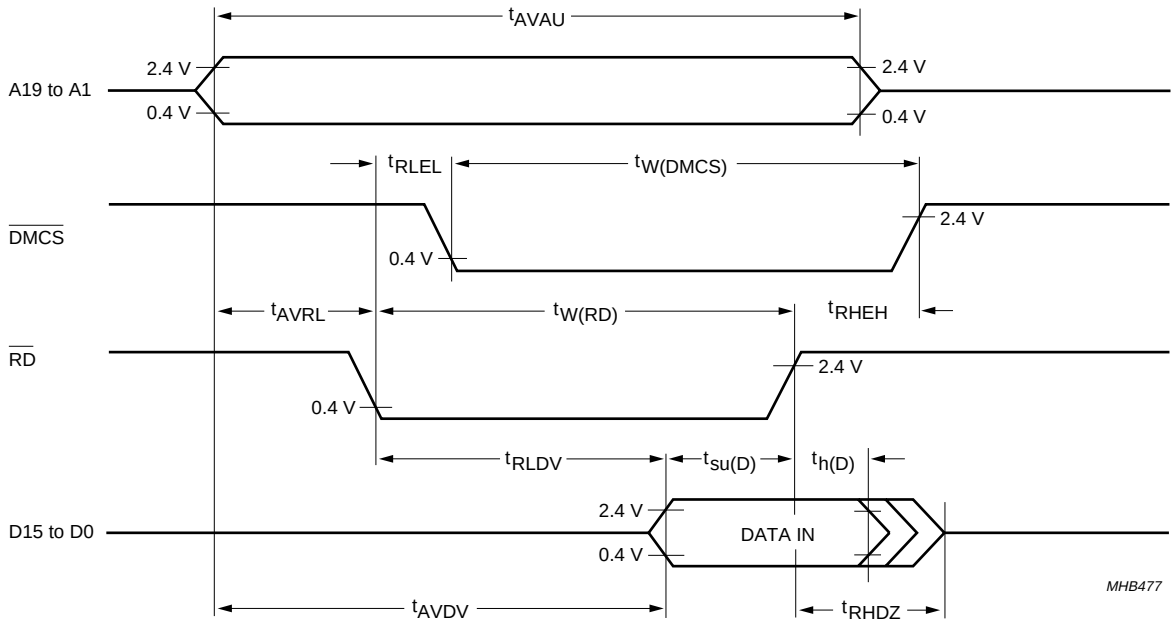
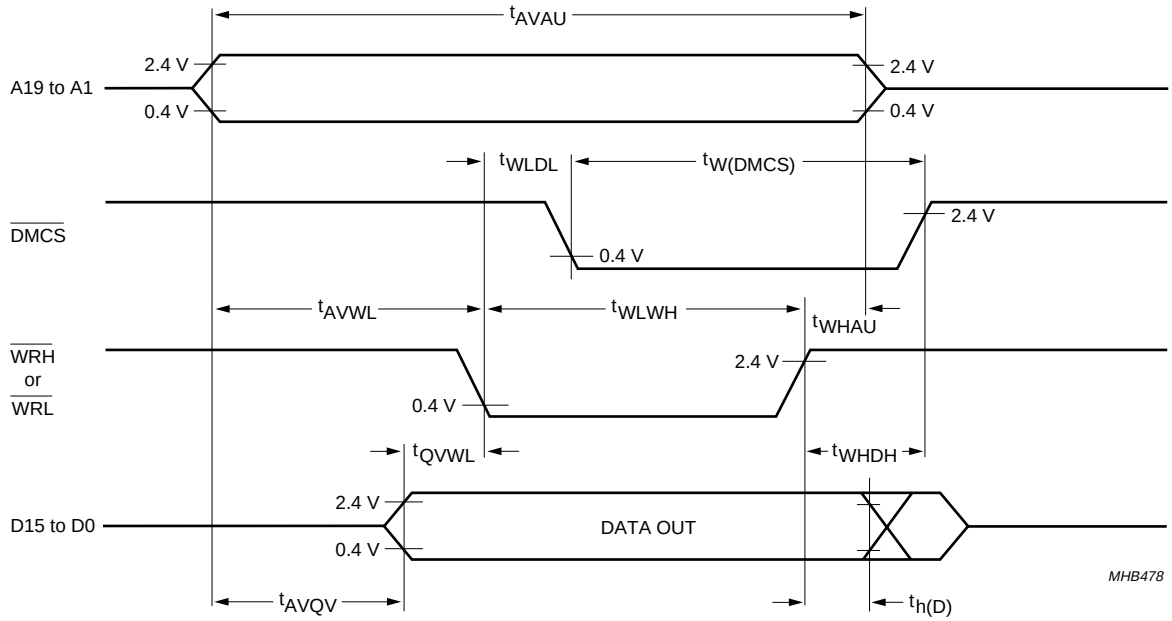


Fig.17 External program memory read cycle (burst).



Default $\overline{\text{DMCS}}$ operation.

Fig.18 External data memory read cycle.



Default $\overline{\text{DMCS}}$ operation.

Fig.19 External data memory write cycle.

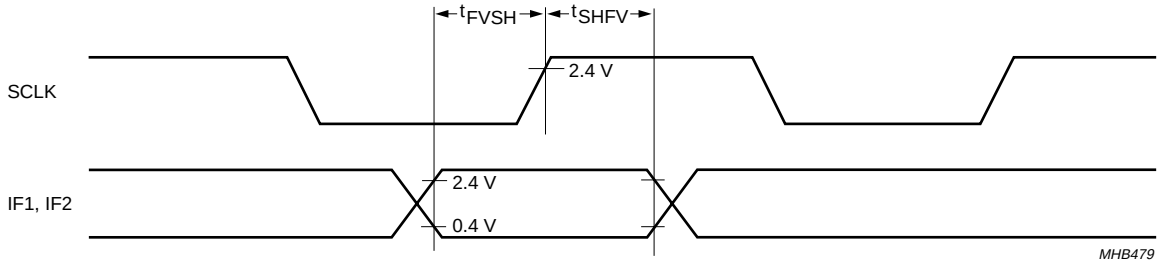
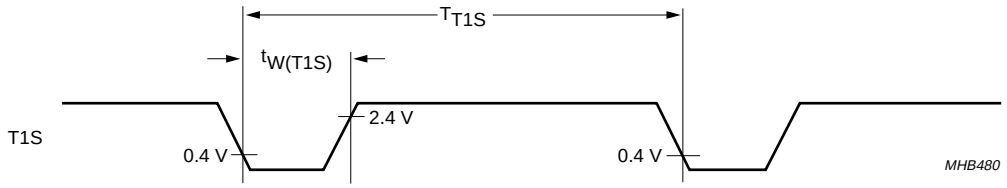


Fig.20 IF input timing.



Signal may be inverted under firmware control.

Fig.21 T1S output pulse timing.

12 DEFAULT APPLICATION AND DEMONSTRATION BOARD

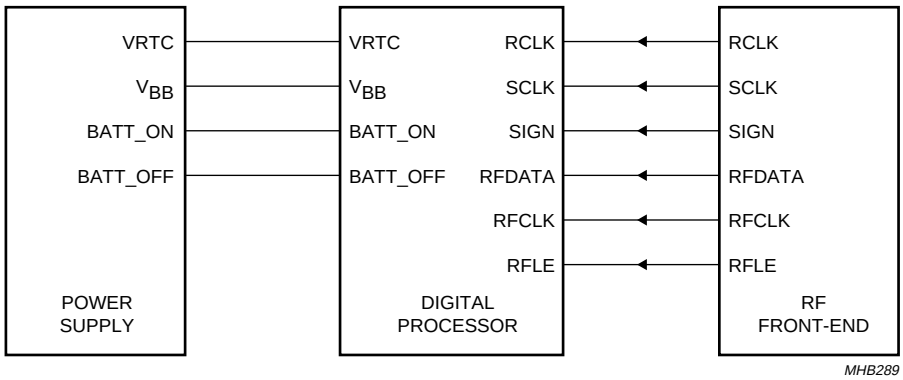


Fig.22 Overall schematic.

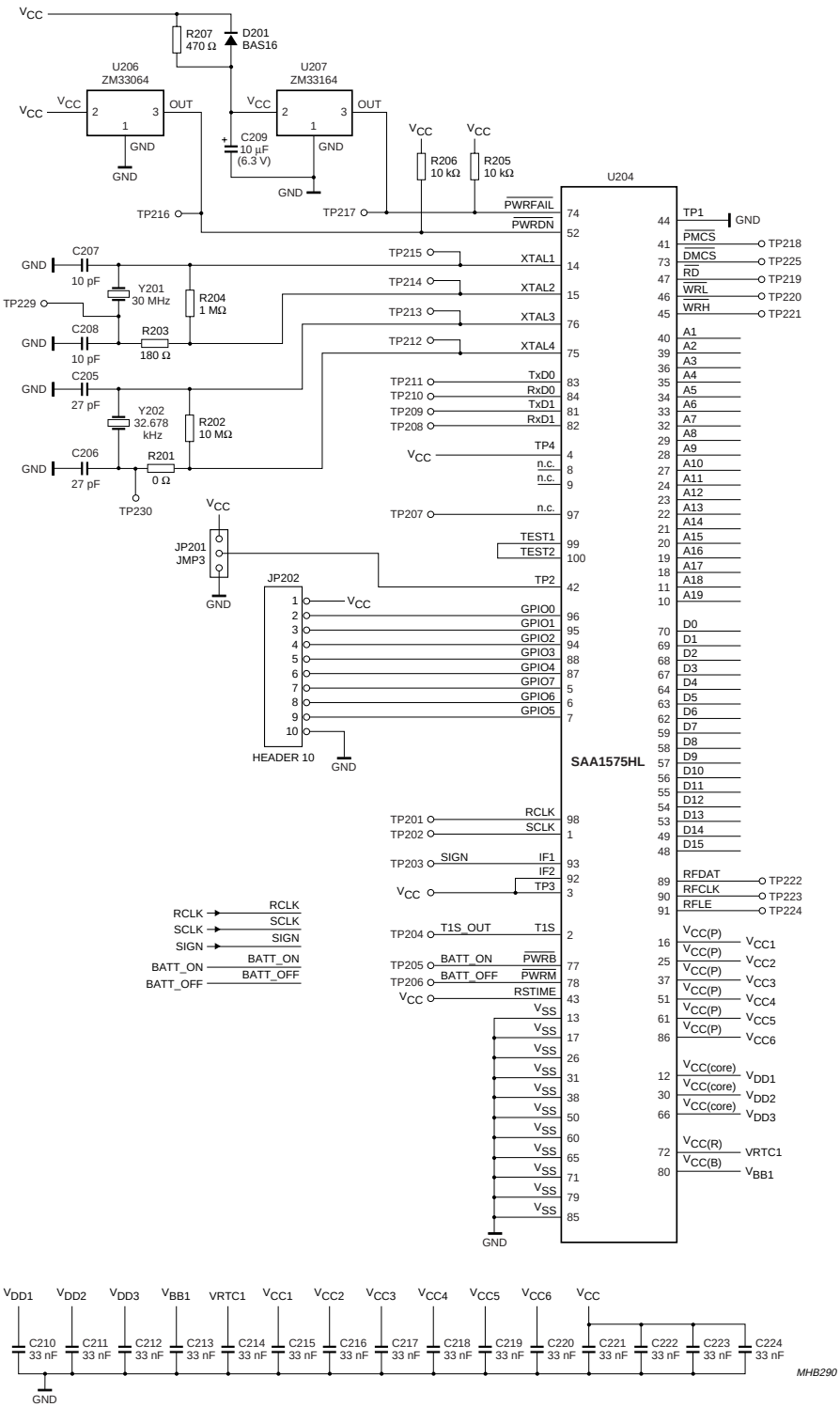


Fig.23 Baseband circuitry (continued in Fig.24).

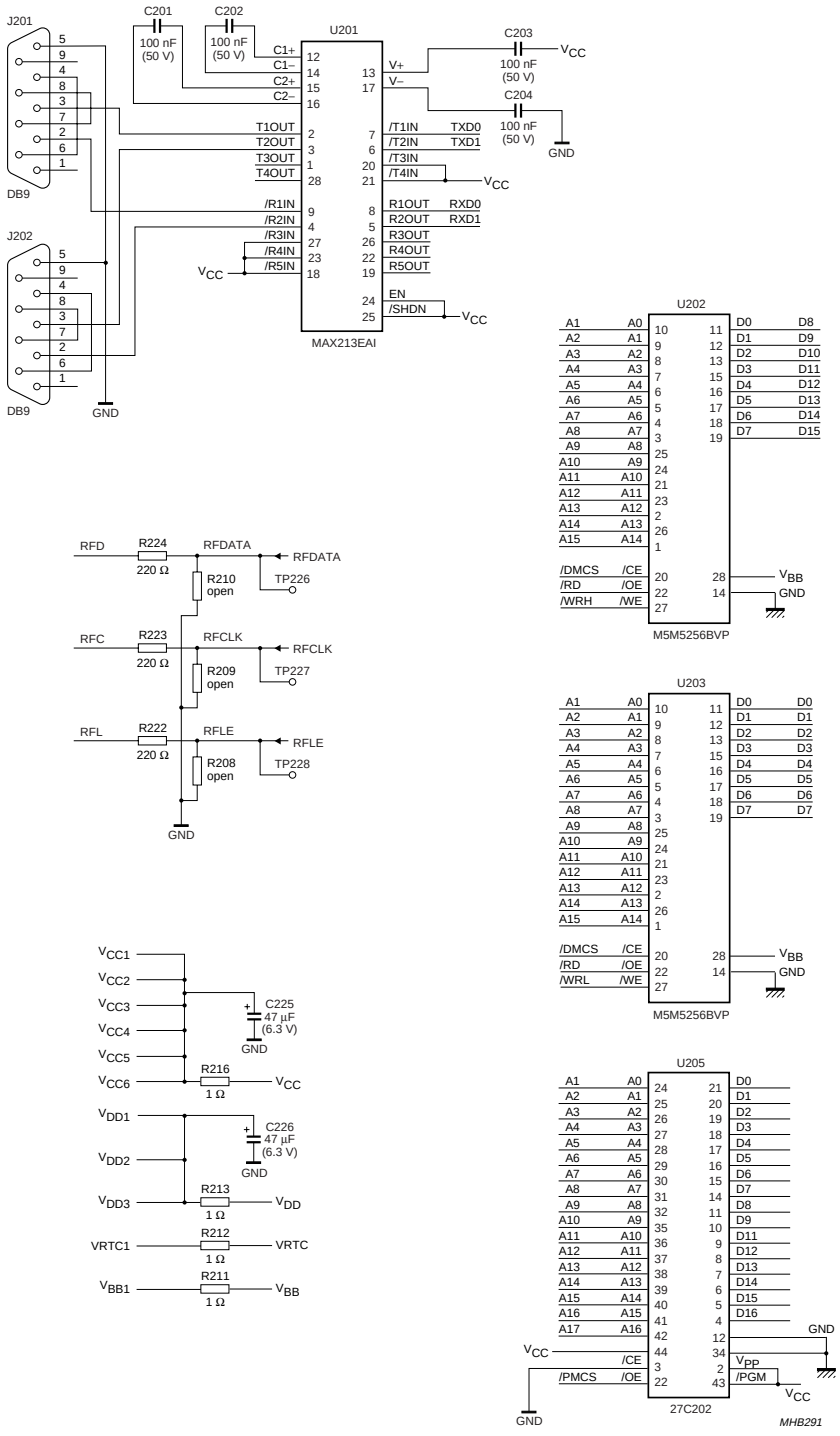


Fig.24 Baseband circuitry (continued from Fig.23).

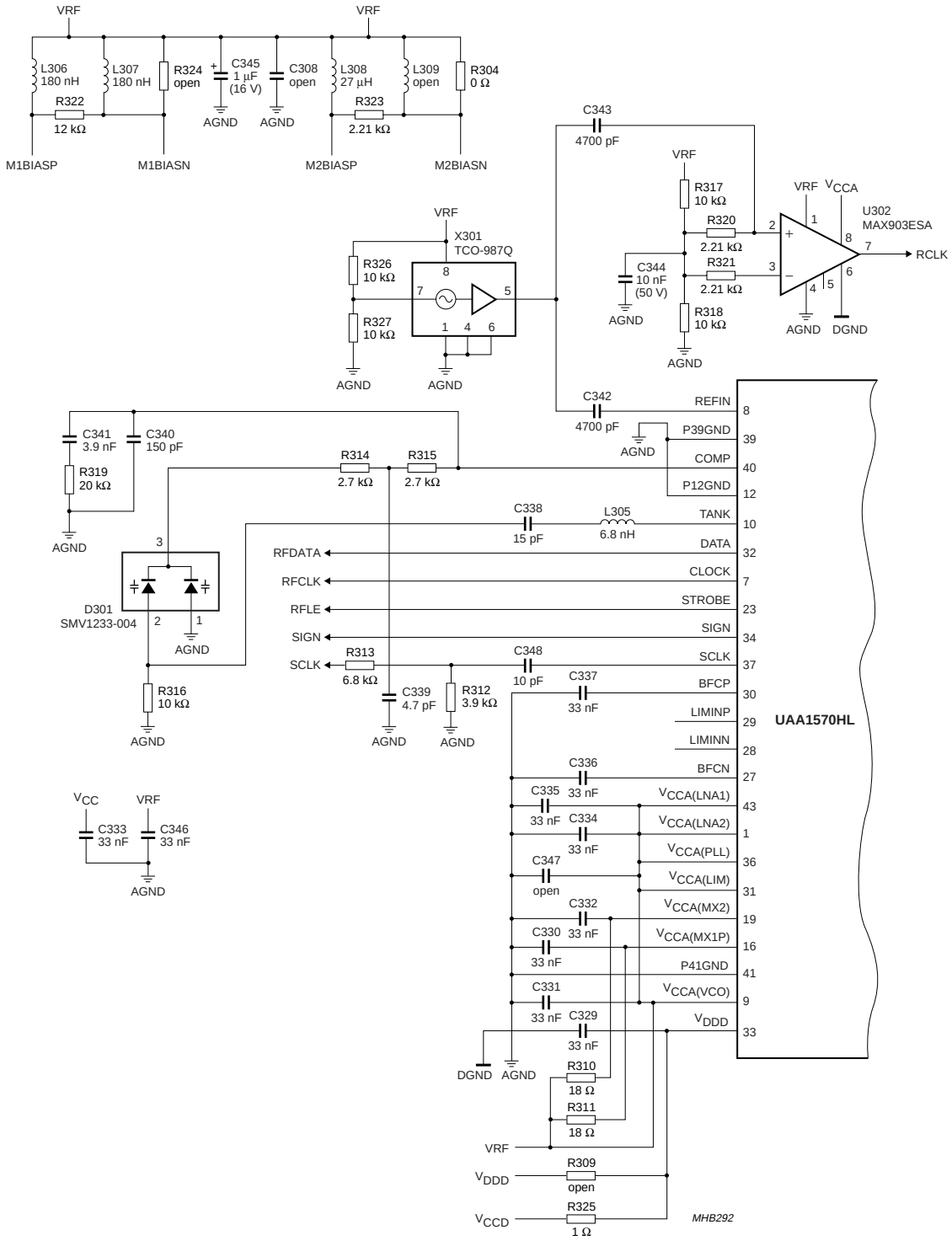


Fig.25 RF front-end circuit (continued in Fig.26).

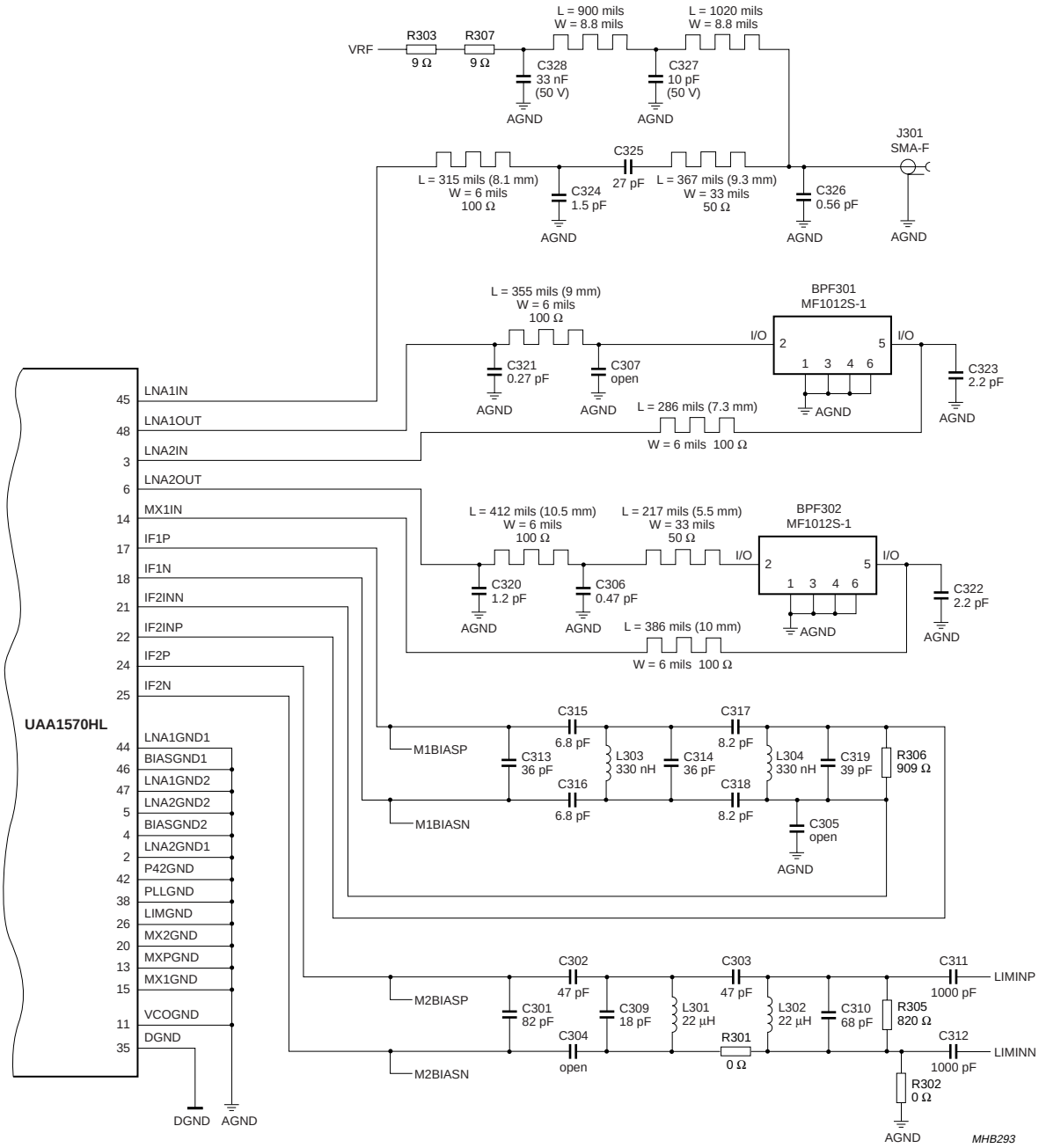


Fig.26 RF front-end circuit (continued from Fig.25).

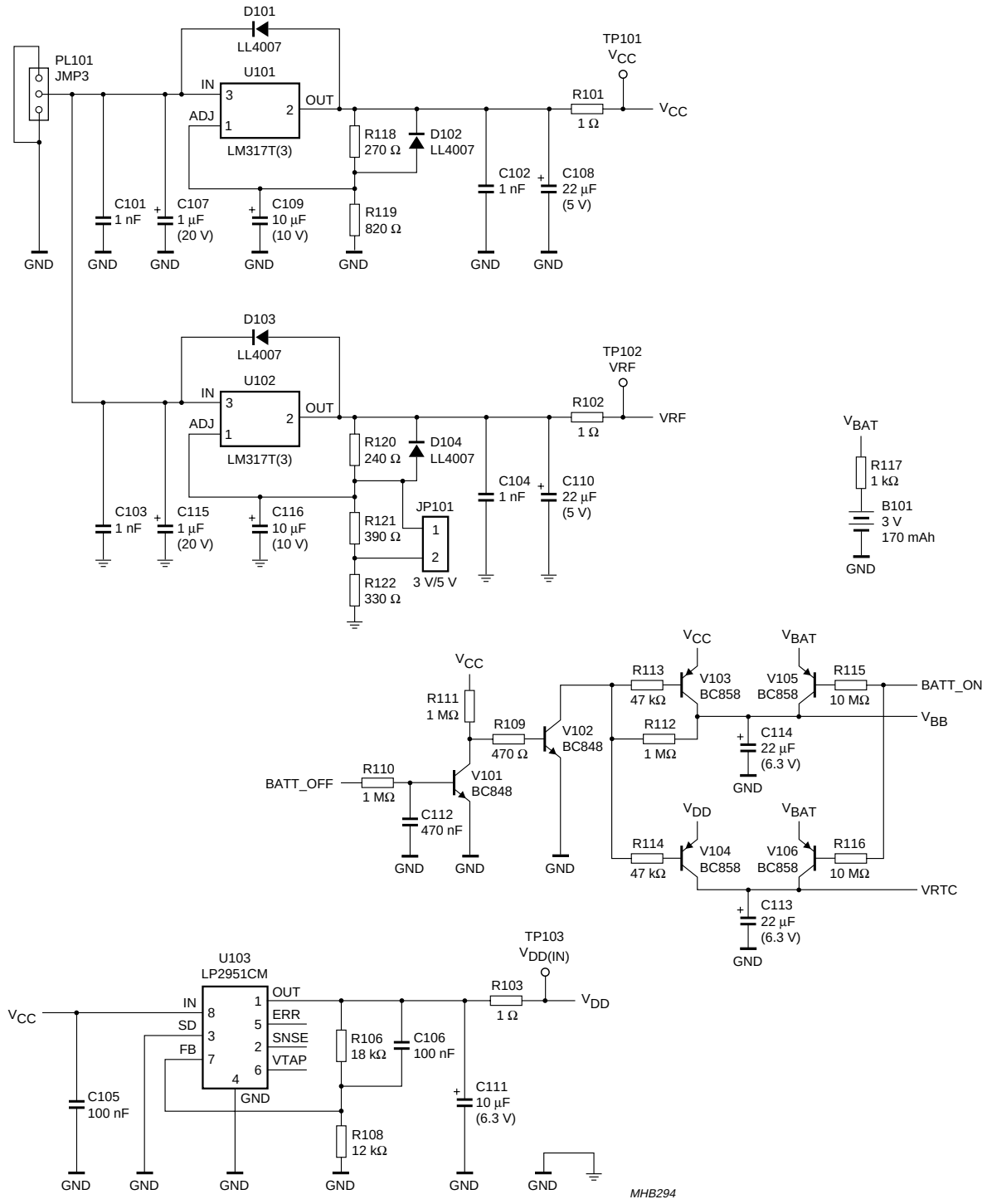


Fig.27 Power supply circuitry.

The GPS system application demonstration board consists of 6 layers with a total final thickness of 1.5 mm. The PCB material is FR4.

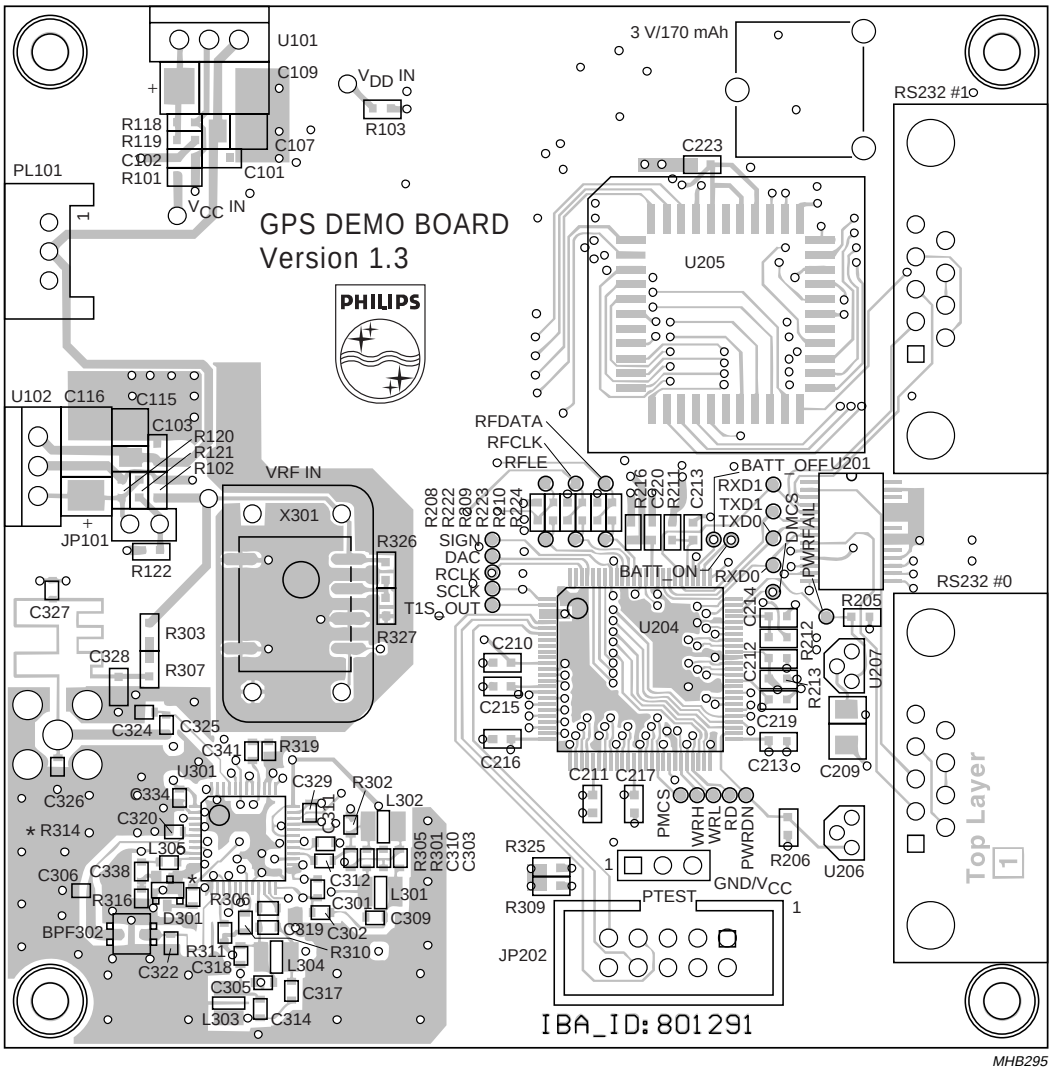


Fig.28 Demonstration board top layer plus components (real size 88.9 mm × 88.9 mm).

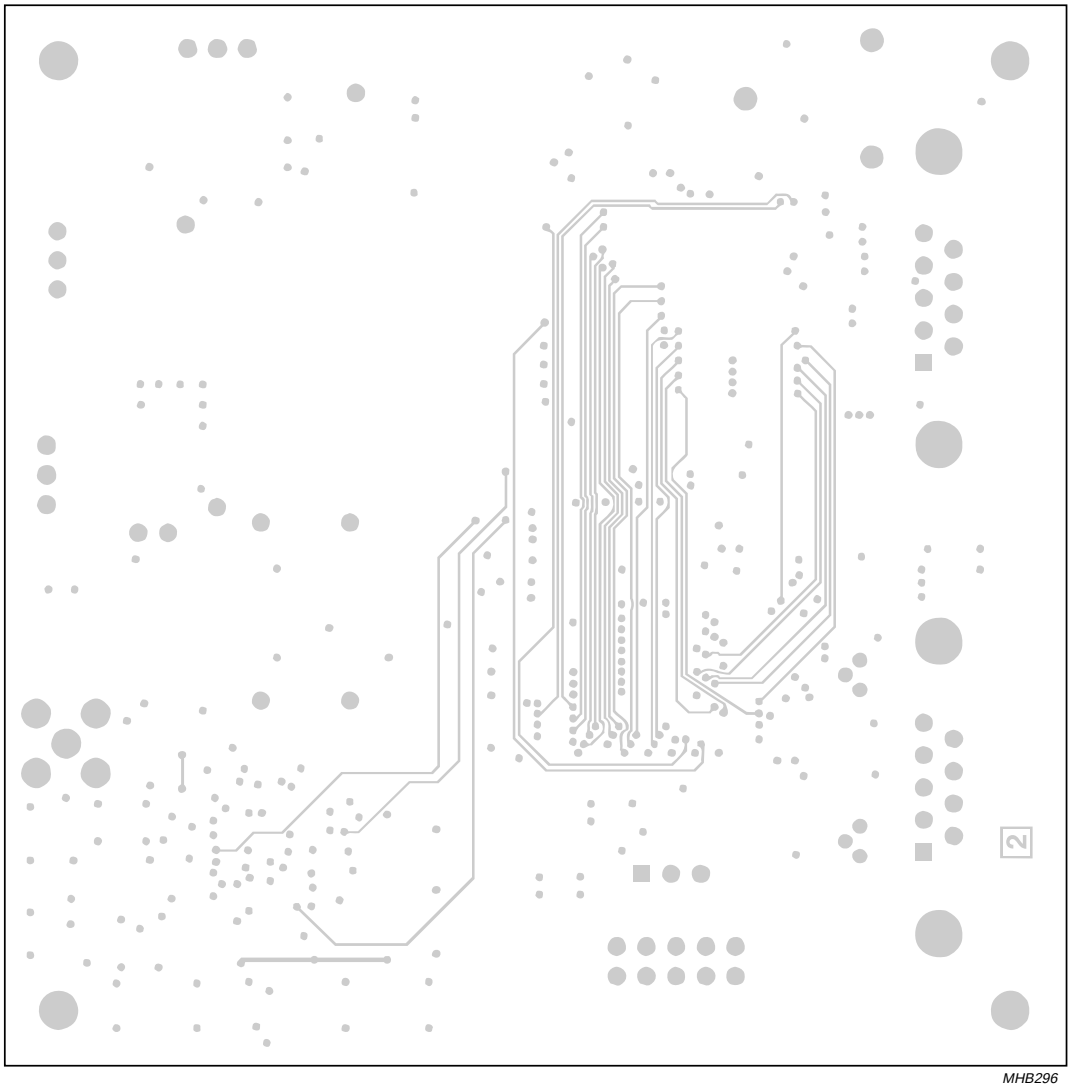


Fig.29 Demonstration board 2nd layer.

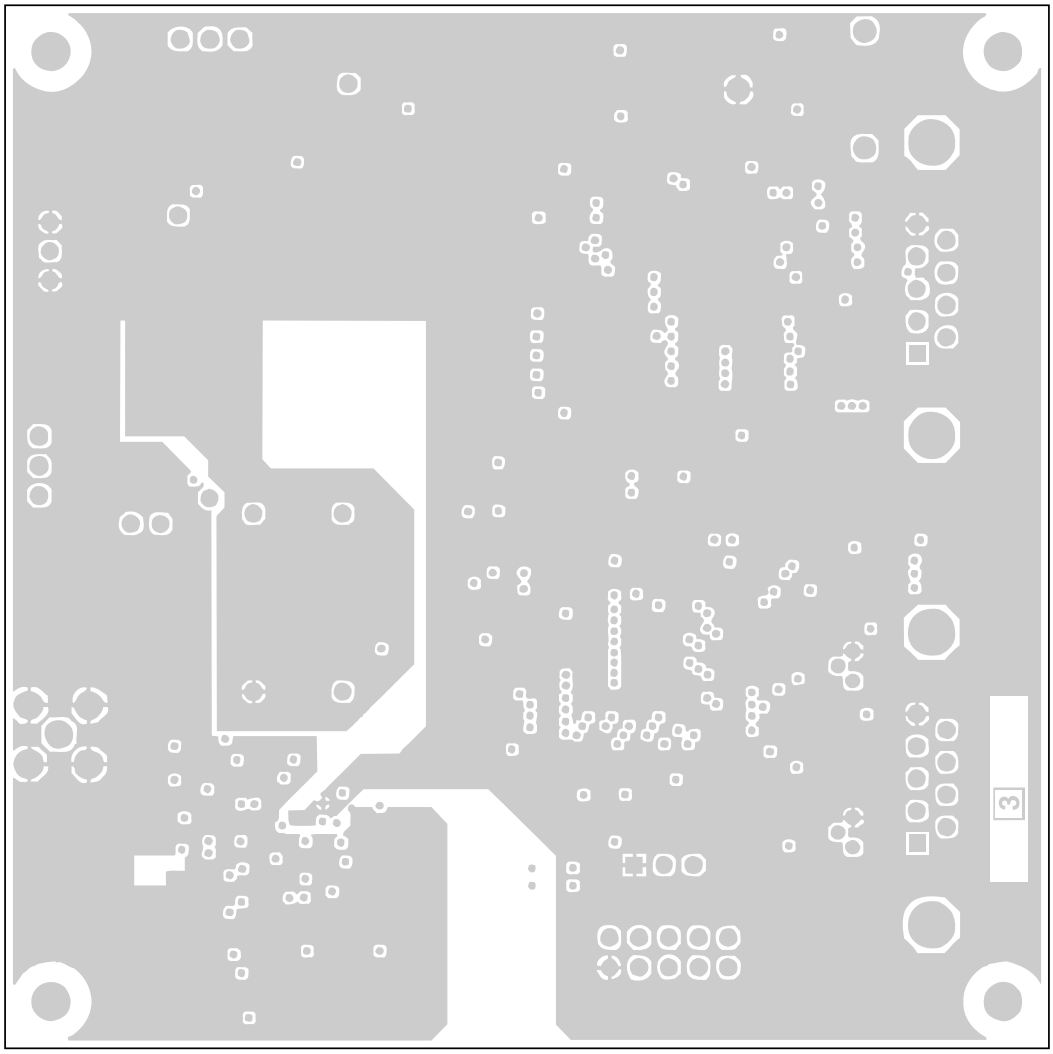


Fig.30 Demonstration board 3rd layer.

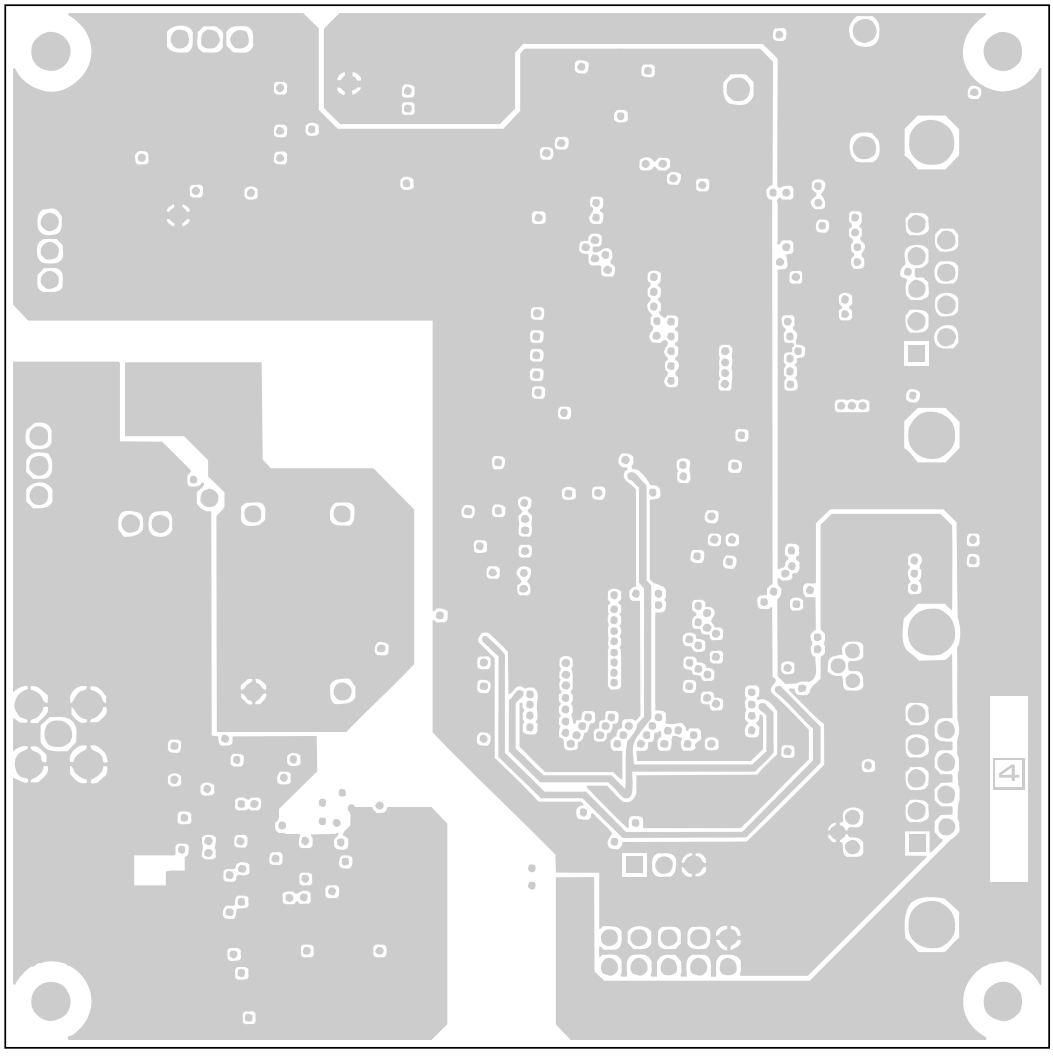
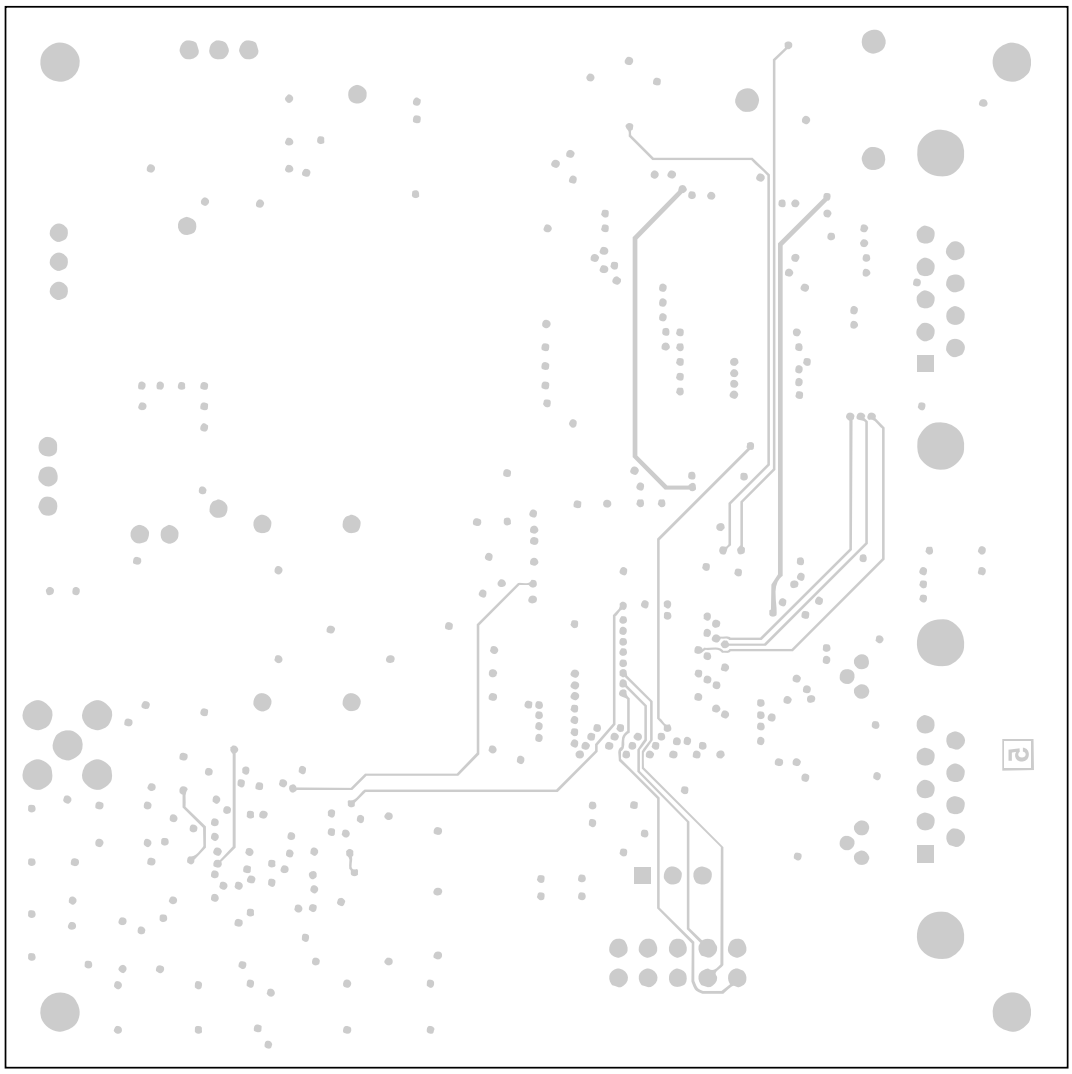


Fig.31 Demonstration board 4th layer.



MHB299

Fig.32 Demonstration board 5th layer.

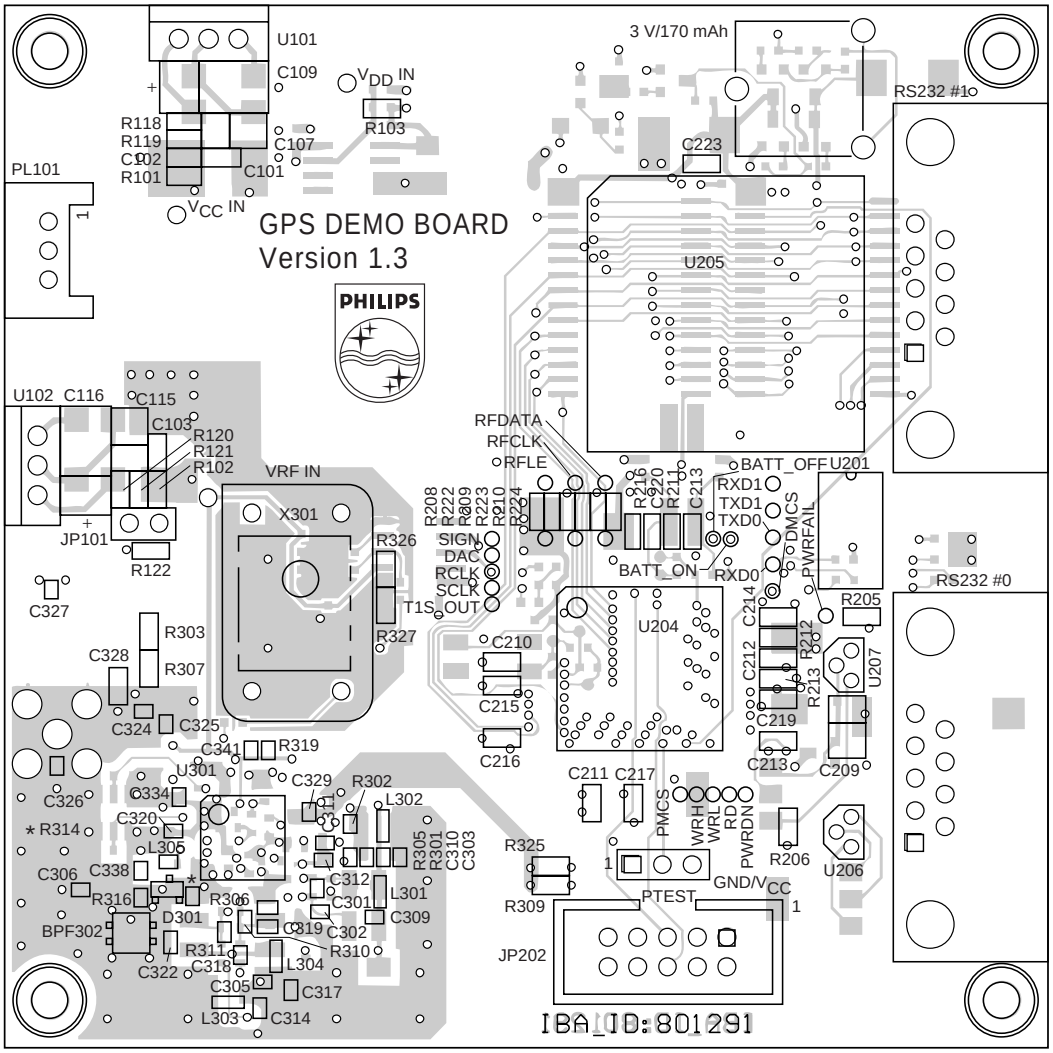


Fig.33 Demonstration board bottom layer plus components.

Table 5 Component list for GPS demonstration board

COMPONENT	TYPE	COMPONENT CHARACTERISTICS		
		VALUE	TOLERANCE	PACKAGE
B101	Lithium battery	3 V/170 mAh	–	CR1/3
C101 to C104, C311 and C312	ceramic capacitor	1 nF/50 V	10%	603
C105, C106, C201 to C204	ceramic capacitor	100 nF/50 V	20%	603
C107 and C115	ceramic capacitor	1 μF/63 V	20%	1210
C108 and C110	tantalum capacitor	22 μF/16 V	20%	–
C109 and C116	tantalum capacitor	10 μF/16 V	20%	–
C111 and C209	tantalum capacitor	10 μF/6.3 V	20%	–
C112	ceramic capacitor	470 nF/63 V	20%	1206
C113 and C114	tantalum capacitor	22 μF/6.3 V	20%	–
C205, C206 and C325	ceramic capacitor	27 pF/50 V	5%	603
C207, C208, C327 and C348	ceramic capacitor	10 pF/50 V	5%	603
C210 to C224, C328 to C337 and C346	ceramic capacitor	33 nF/63 V	10%	603
C225 and C226	tantalum capacitor	47 μF/6.3 V	20%	–
C301	ceramic capacitor	82 pF/50 V	5%	603
C302 and C303	ceramic capacitor	47 pF/50 V	5%	603
C304, C305, C307, C308 and C347	–	not loaded	–	–
C306	ceramic capacitor	0.47 pF/50 V	±0.1 pF	603
C309	ceramic capacitor	18 pF/50 V	5%	603
C310	ceramic capacitor	68 pF/50 V	5%	603
C313 and C314	ceramic capacitor	36 pF/50 V	5%	603
C315 and C316	ceramic capacitor	6.8 pF/50 V	±0.25 pF	603
C317 and C318	ceramic capacitor	8.2 pF/50 V	±0.25 pF	603
C319	ceramic capacitor	39 pF/50 V	5%	603
C320	ceramic capacitor	1.2 pF/50 V	±0.25 pF	603
C321	ceramic capacitor	0.27 pF/50 V	±0.1 pF	603
C322 and C323	ceramic capacitor	2.2 pF/50 V	±0.25 pF	603
C324	ceramic capacitor	1.5 pF/50 V	±0.25 pF	603
C326	ceramic capacitor	0.56 pF/50 V	±0.1 pF	603
C338	ceramic capacitor	15 pF/50 V	5%	603
C339	ceramic capacitor	4.7 pF/50 V	±0.25 pF	603
C340	ceramic capacitor	150 pF/50 V	5%	603
C341	ceramic capacitor	3.9 nF/50 V	10%	603
C342 and C343	ceramic capacitor	4.7 nF/50 V	5%	603
C344	ceramic capacitor	10 nF/50 V	10%	603
C345	tantalum capacitor	1 μF/16 V	20%	–
D101 to D104	LL4007 diode, equivalent to 1N4007	–	–	–
D201	SMD diode BAS 16	–	–	SOT23

COMPONENT	TYPE	COMPONENT CHARACTERISTICS		
		VALUE	TOLERANCE	PACKAGE
D301	Alpha SMV1204-133 varactor	–	–	SOT23
L301 and L302	SMD inductor	22 μH	5%	1008
L303 and L304	SMD inductor	330 nH	5%	1008
L305	SMD inductor	6.8 nH	±5%	603
L306 and L307	SMD inductor	180 nH	±5%	1008
L308	SMD inductor	27 μH	5%	1008
L309	–	not loaded	–	–
R101, R102, R103, R211, R212, R213, R216 and R325	SMD resistor	1 Ω	5%	603
R106	SMD resistor	18 kΩ	5%	603
R108 and R322	SMD resistor	12 kΩ	1%	603
R109 and R207	SMD resistor	470 Ω	1%	603
R110, R111, R112 and R204	SMD resistor	1 MΩ	1%	603
R113 and R114	SMD resistor	47 kΩ	1%	603
R115, R116 and R202	SMD resistor	10 MΩ	1%	603
R117	SMD resistor	1 kΩ	1%	603
R118	SMD resistor	270 Ω	1%	603
R119 and R305	SMD resistor	820 Ω	1%	603
R120	SMD resistor	240 Ω	1%	603
R121	SMD resistor	390 Ω	1%	603
R122	SMD resistor	330 Ω	1%	603
R201, R301, R302 and R304	SMD resistor	0 Ω	–	603
R203	SMD resistor	180 Ω	5%	603
R205, R206, R316, R317, R318, R326 and R327	SMD resistor	10 kΩ	1%	603
R208, R209, R210, R309 and R324	–	not loaded	–	–
R222 to R224	SMD resistor	220 Ω	5%	603
R303 and R307	SMD resistor	9.1 Ω	5%	603
R306	SMD resistor	910 Ω	1%	603
R310 and R311	SMD resistor	18 Ω	1%	603
R312	SMD resistor	3.9 kΩ	1%	603
R313	SMD resistor	6.8 kΩ	1%	603
R314 and R315	SMD resistor	2.7 kΩ	1%	603
R319	SMD resistor	20 kΩ	5%	603
R320, R321 and R323	SMD resistor	2.2 kΩ	1%	603
U101 and U102[1]	LM317T voltage regulator	–	–	TO220
U103	LP2951CM voltage regulator (National)	–	–	SO8

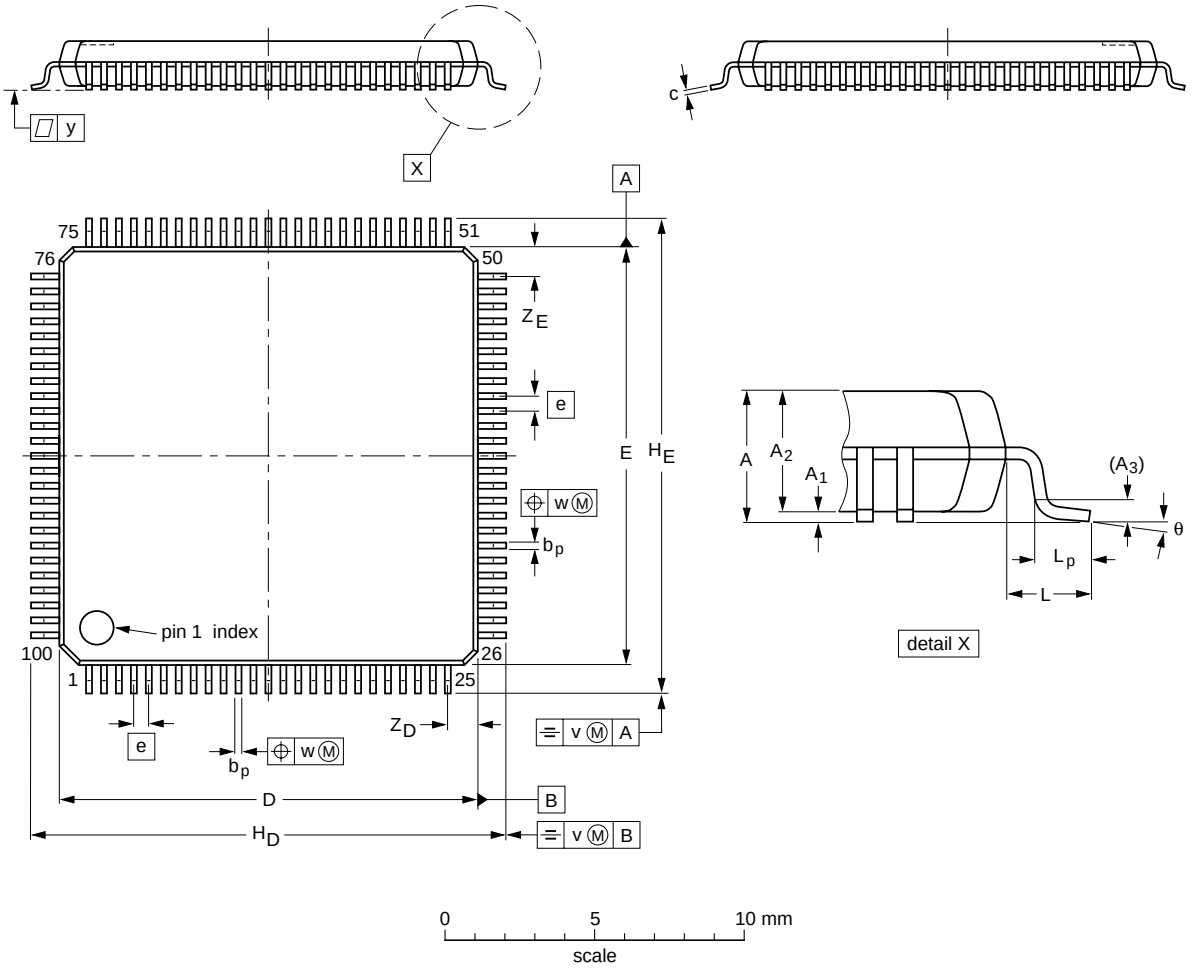
COMPONENT	TYPE	COMPONENT CHARACTERISTICS		
		VALUE	TOLERANCE	PACKAGE
U201	MAX213EAIRS2312 transceiver (Maxim)	–	–	SSOP28
U202 and U203	SRAM M5M5256BFP-70LL 32k × 8 (Mitsubishi)	–	–	SO28
U205	27C202 EPROM	–	–	PLCC44
U206	ZM33064 power monitor	–	–	–
U207	ZM33164 power monitor	–	–	–
U302	MAX903ESA comparator (Maxim)	–	–	SO8
V101 and V102	BC848 or BC847C NPN transistor	–	–	SOT23
V103 to V106	BC858 PNP transistor	–	–	SOT23
X301	TCXO TCO-987Q	–	–	–
Y201	30 MHz crystal, 16 pF load capacitance	–	–	–
Y202	SMD crystal	32.768 kHz	±30 ppm	–
BPF301 and BPF302	MF1012S-1 saw filter	–	–	–

Note

1. With heat sink depending on input voltage.

13 PACKAGE OUTLINE

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.5 1.3	0.25	0.28 0.16	0.18 0.12	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.2	0.12	0.1	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1						~~95-12-19~~ 97-08-04

14 SOLDERING

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

15 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

16 LIFE SUPPORT APPLICATIONS

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